

FIG. 1  
PRIOR ART

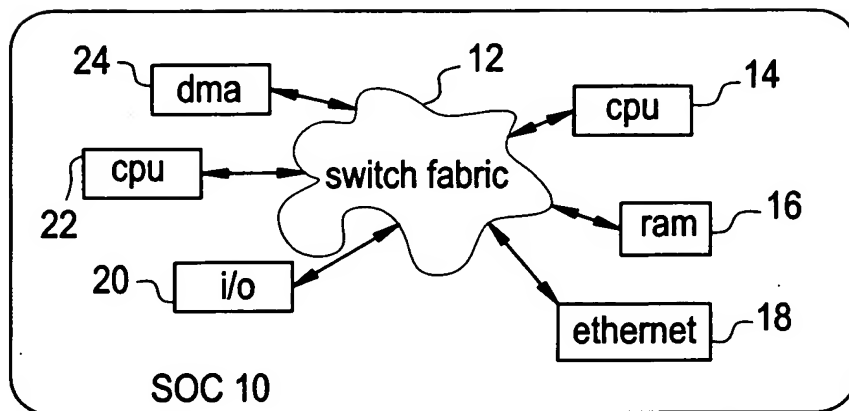


FIG. 2

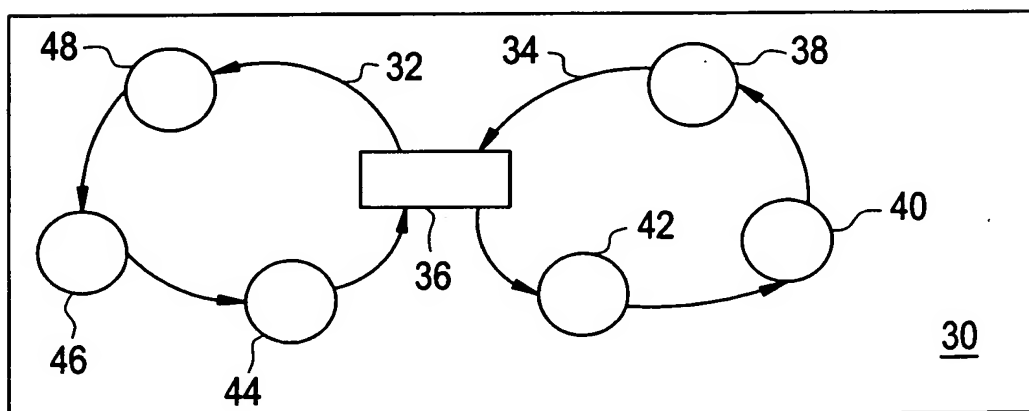




FIG. 3

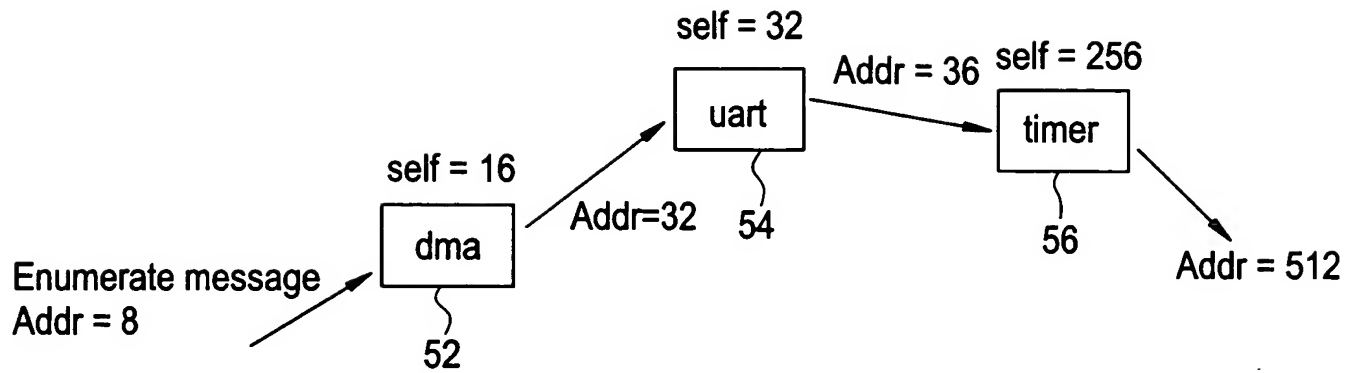


FIG. 4

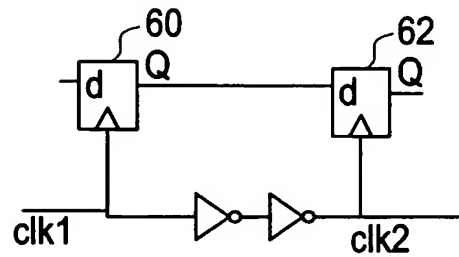


FIG. 5

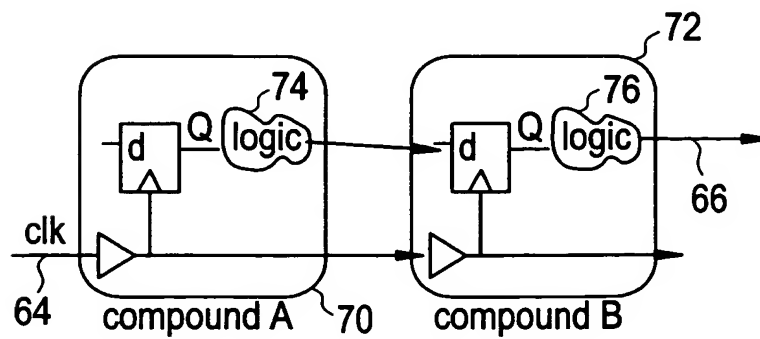


FIG. 6

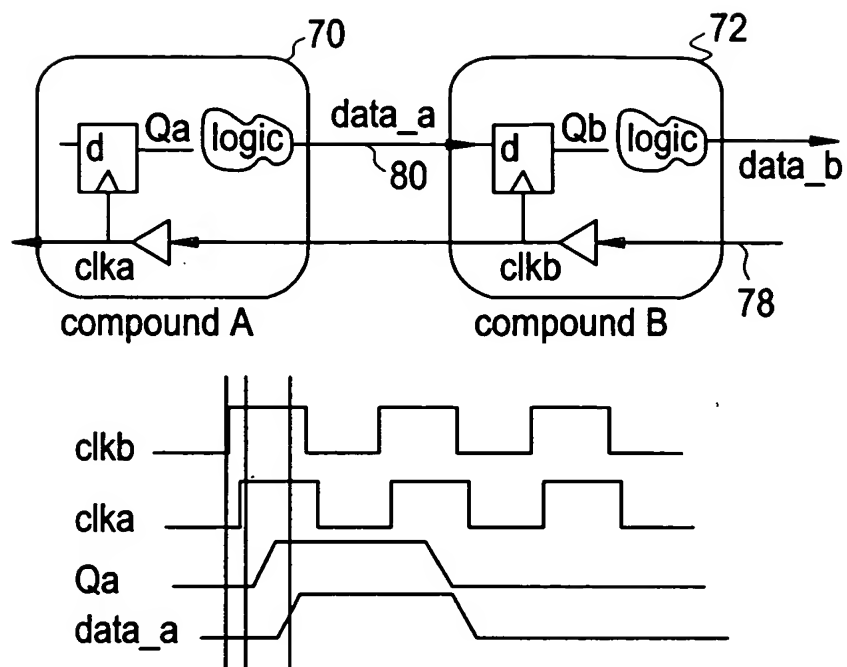
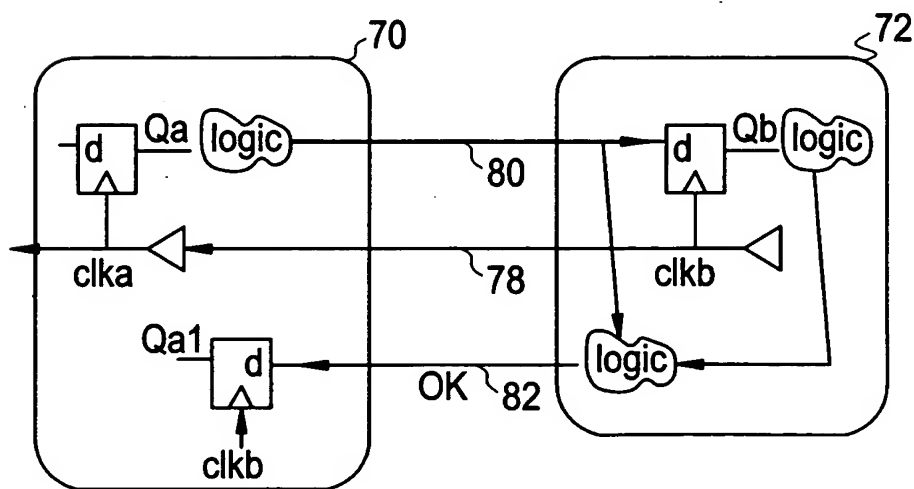


FIG. 7



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FIG. 8

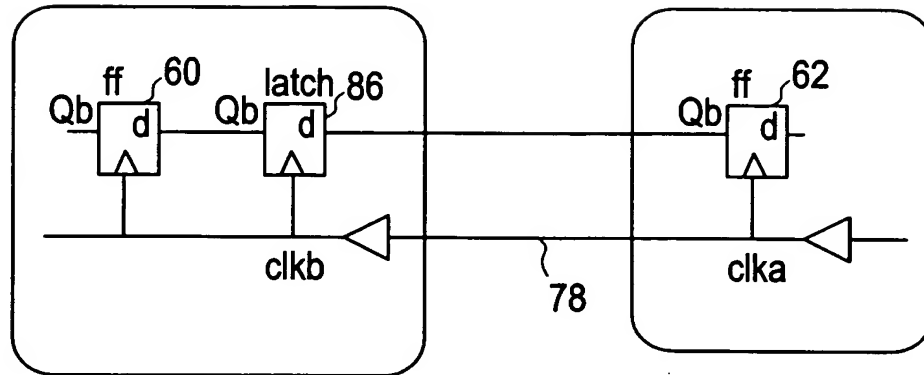
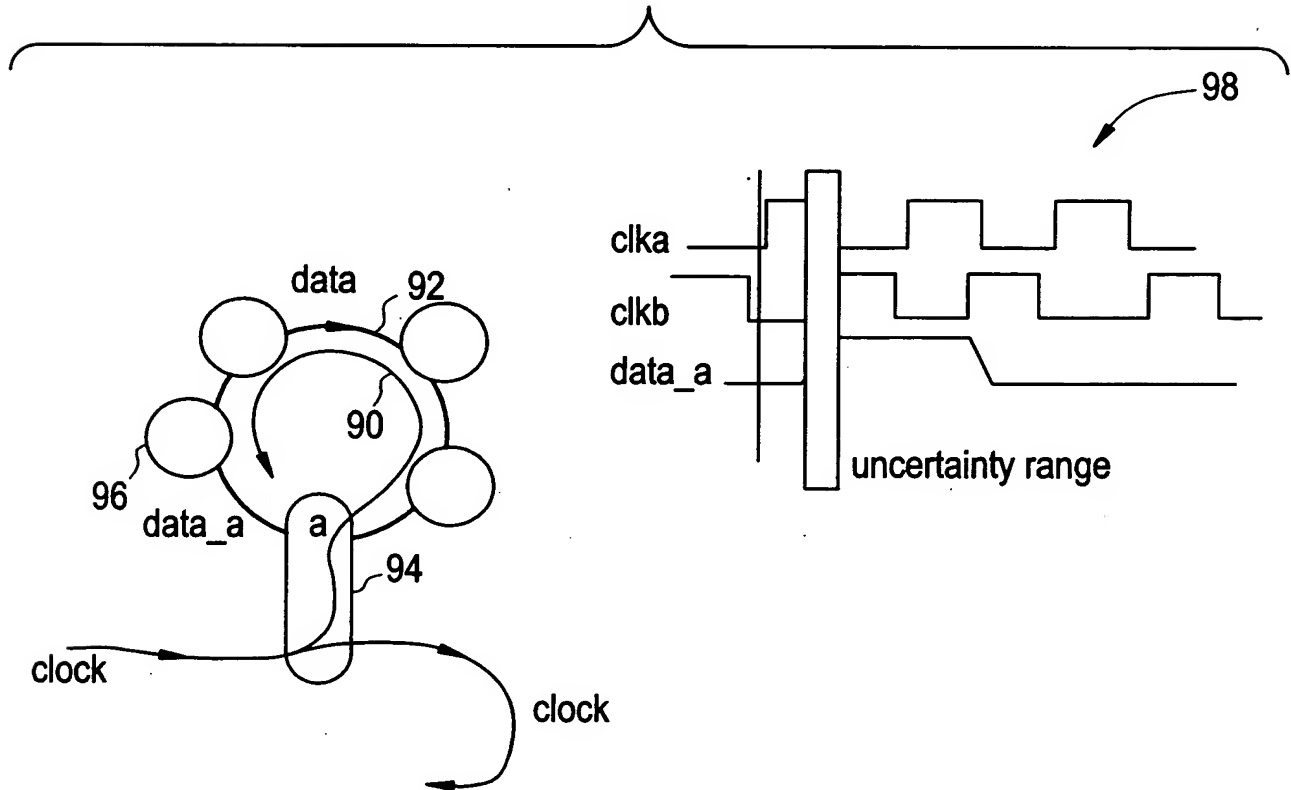


FIG. 9



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FIG. 10

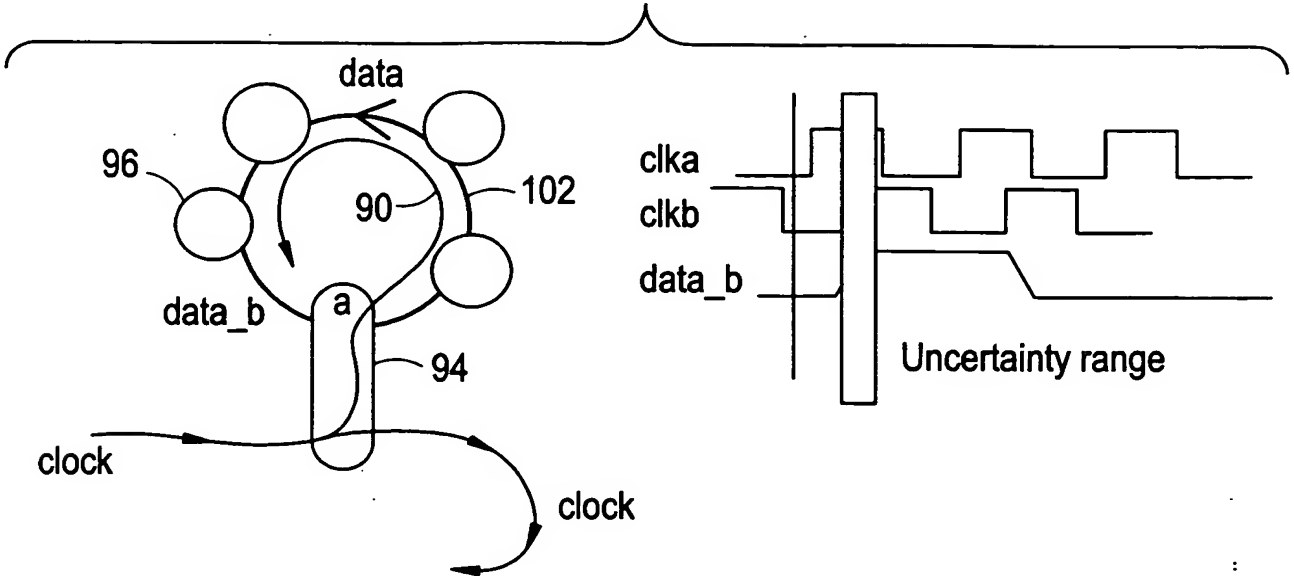


FIG. 11

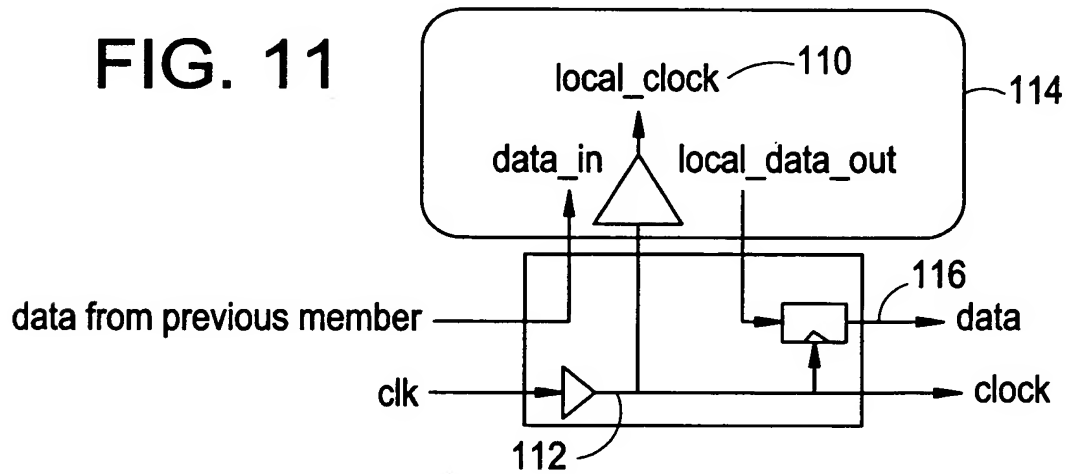


FIG. 12

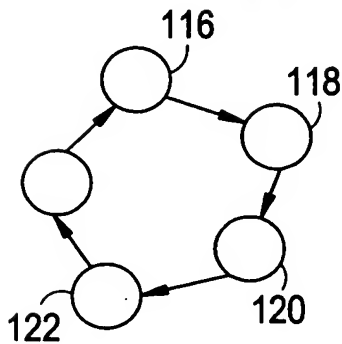


FIG. 13

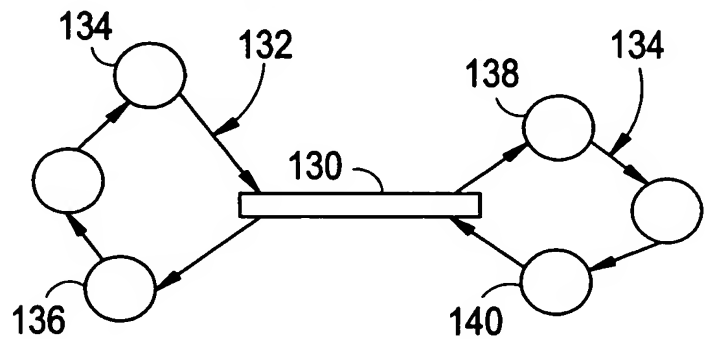


FIG. 14

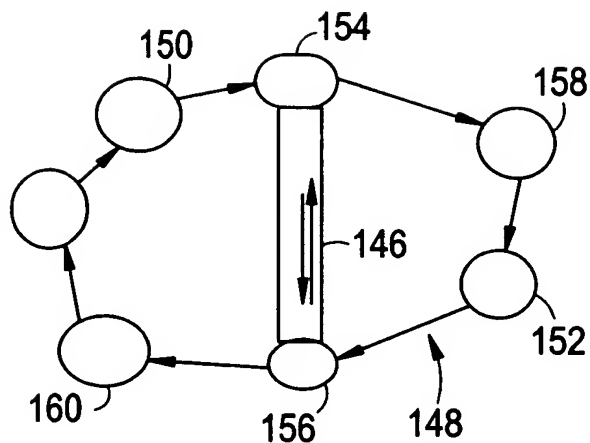


FIG. 15

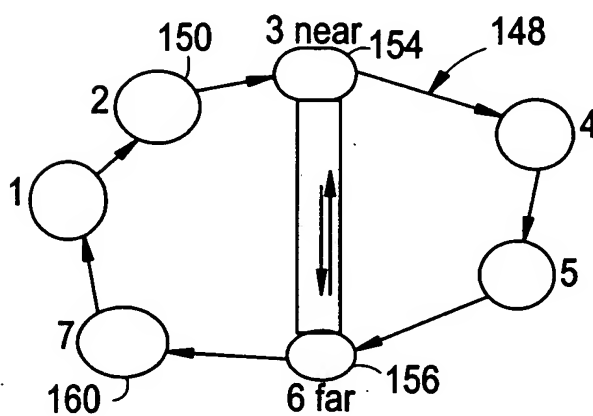


FIG. 16

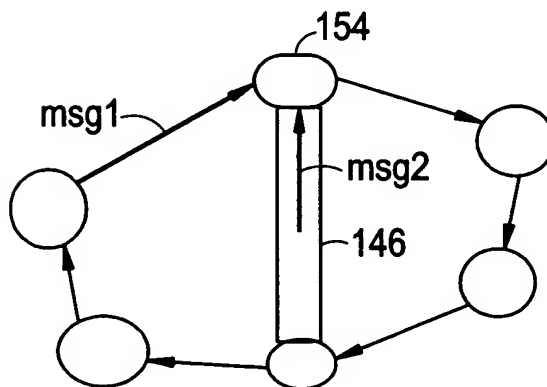


FIG. 17

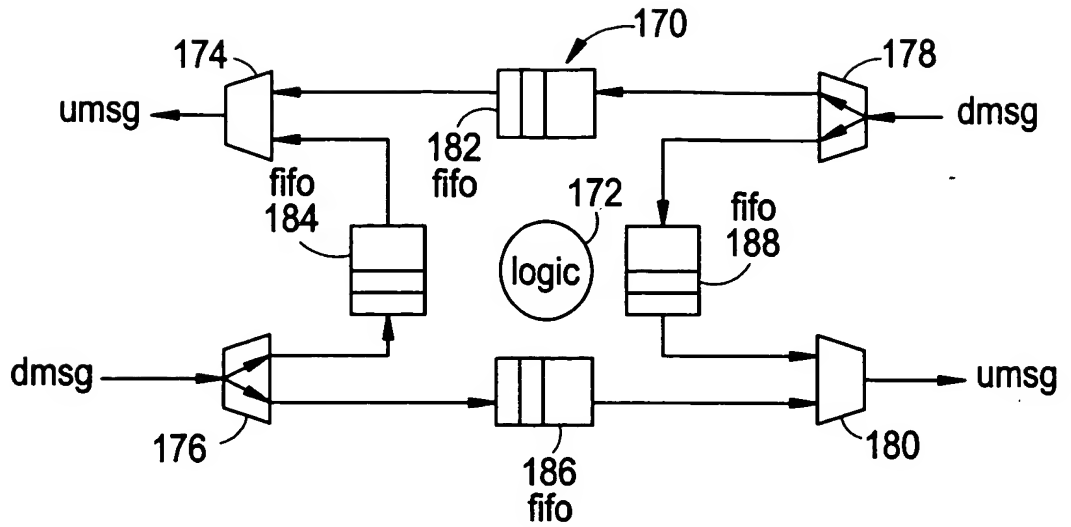


FIG. 18

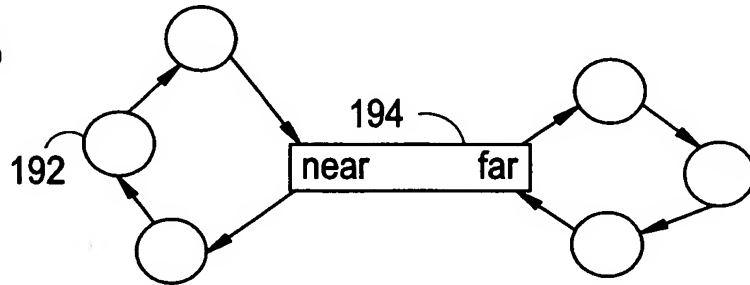


FIG. 19

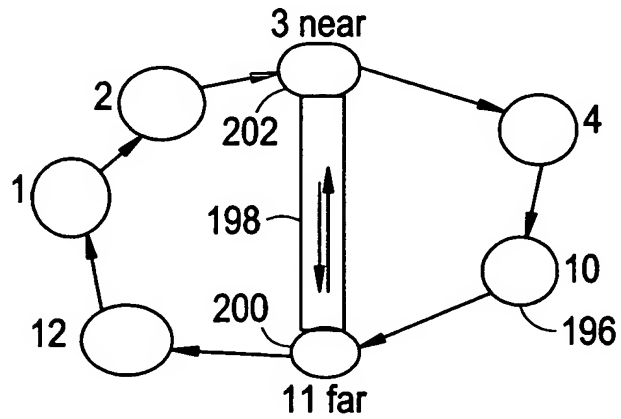


FIG. 20

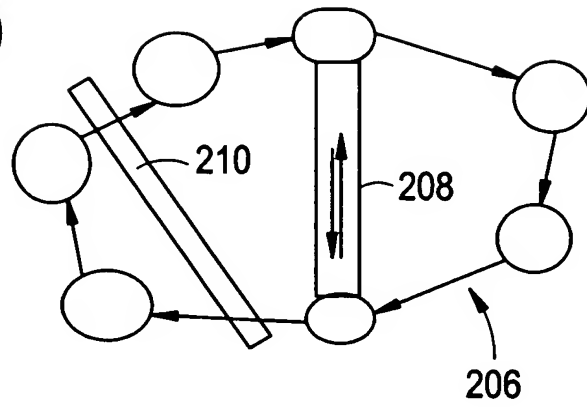


FIG. 21

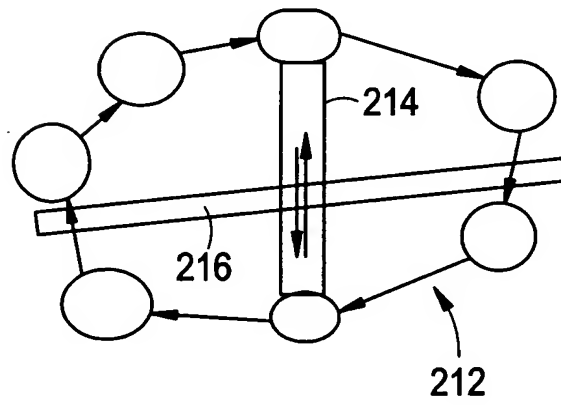


FIG. 22

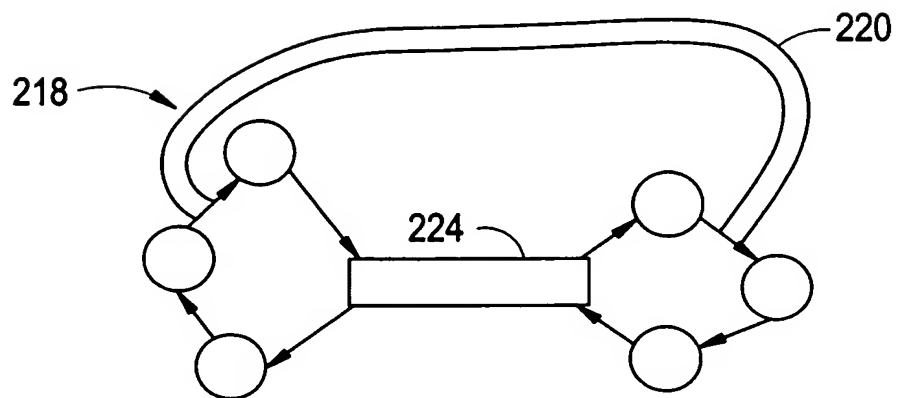




FIG. 23

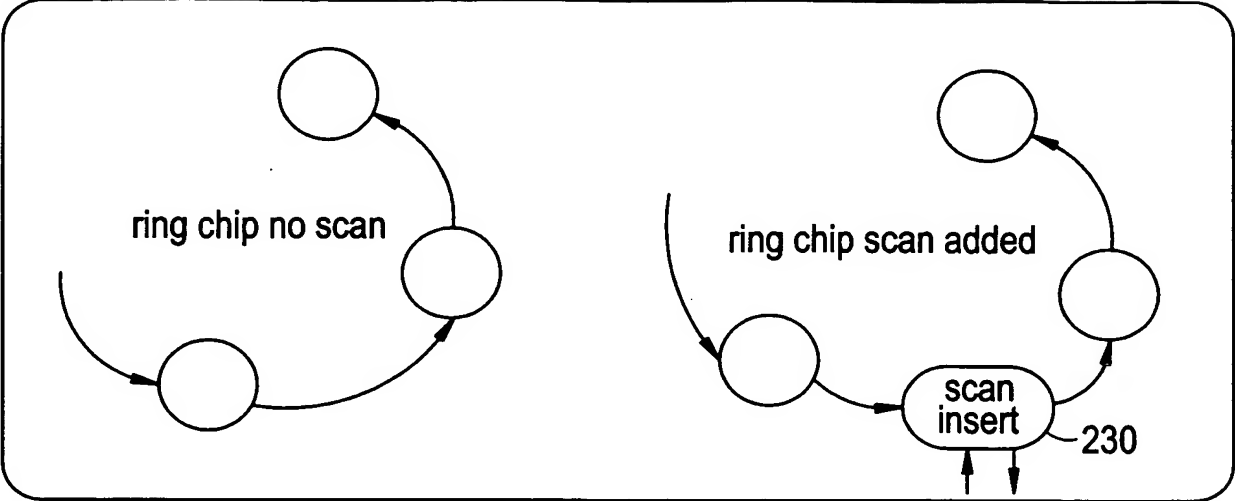


FIG. 24

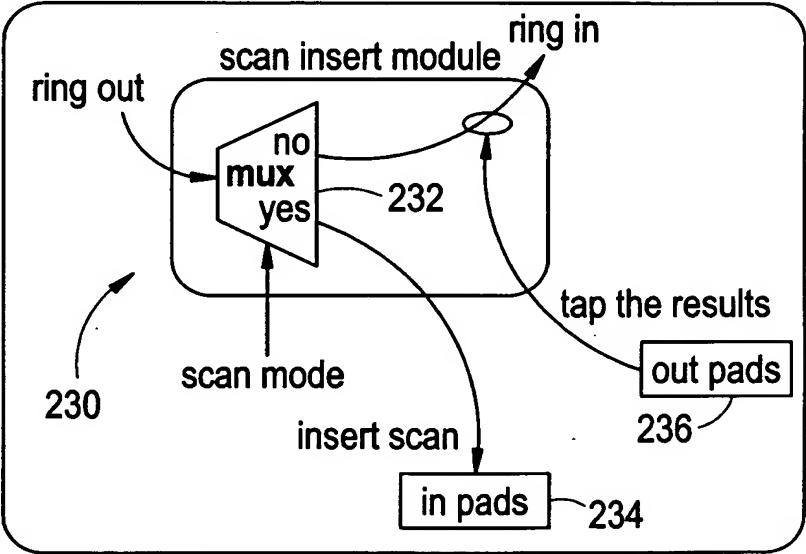


FIG. 25

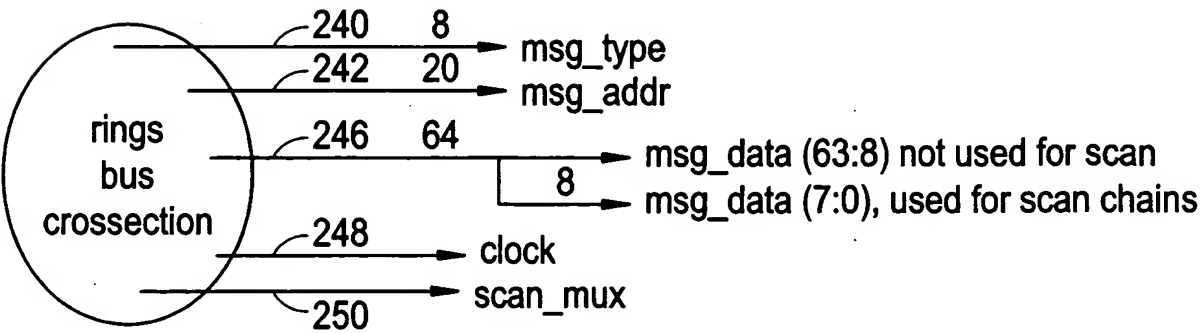


FIG. 26

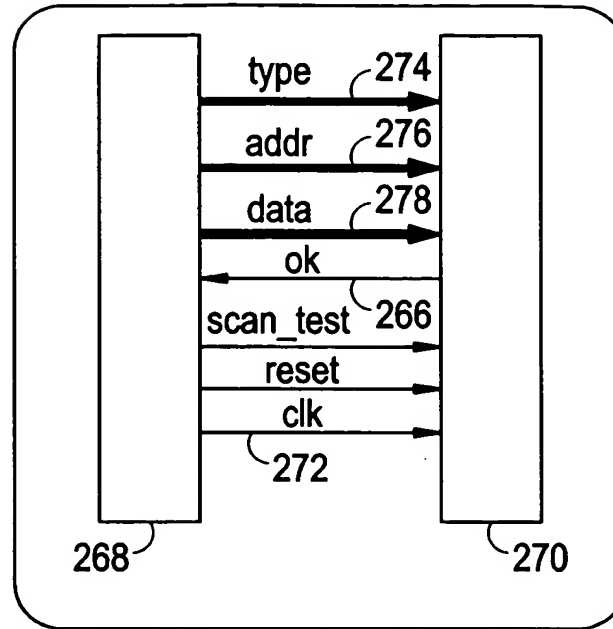
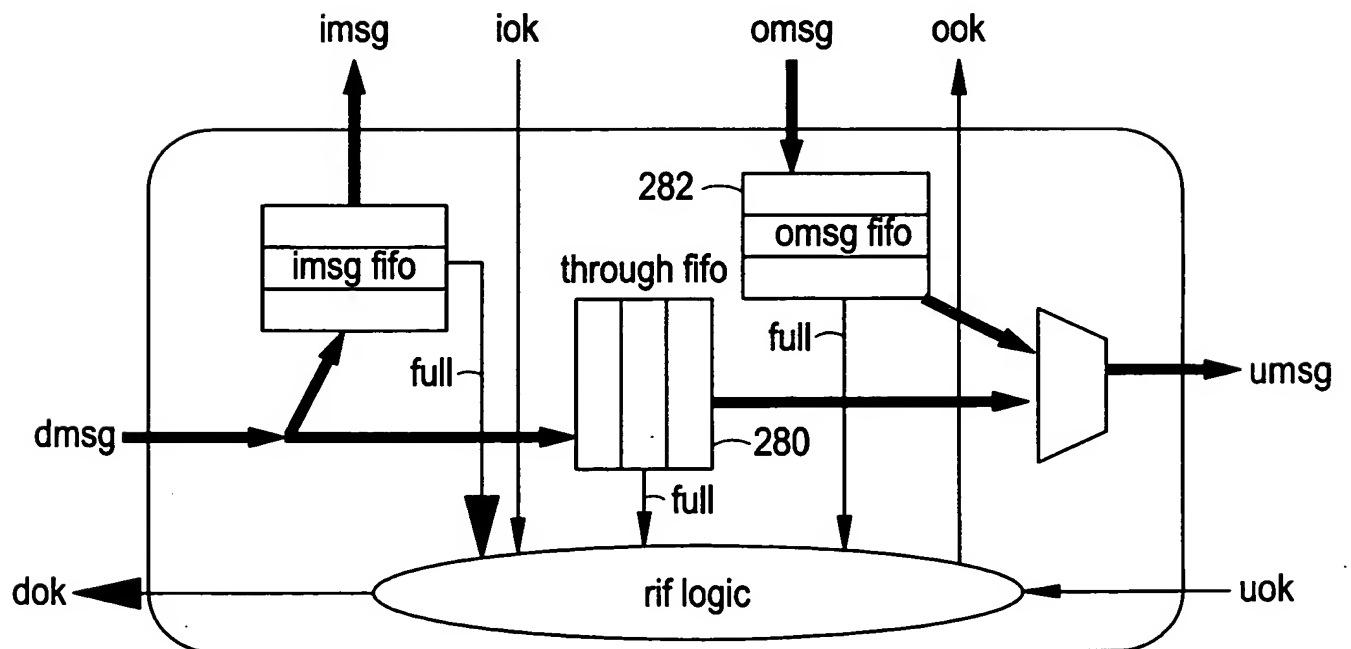


FIG. 27



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FIG. 28

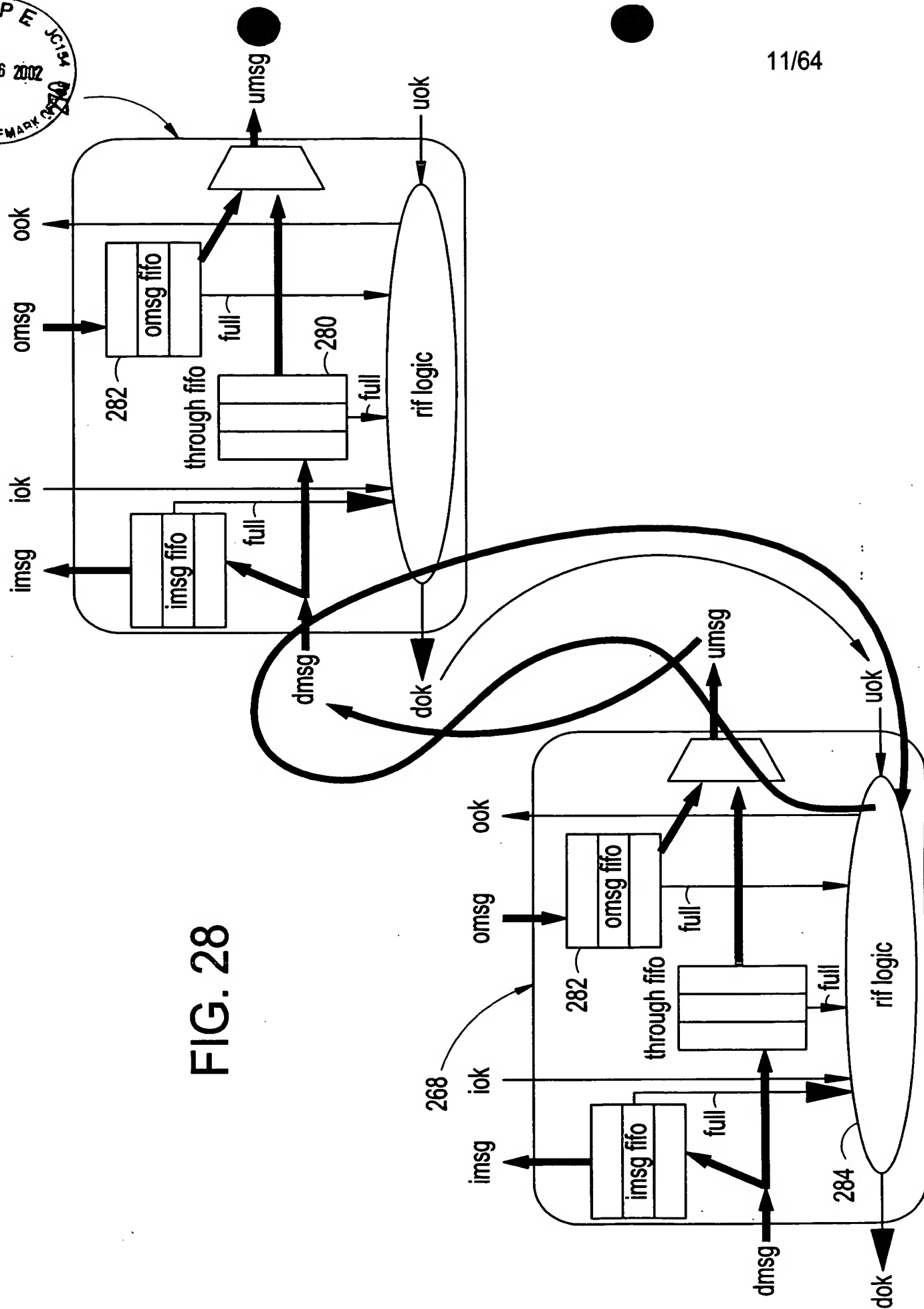
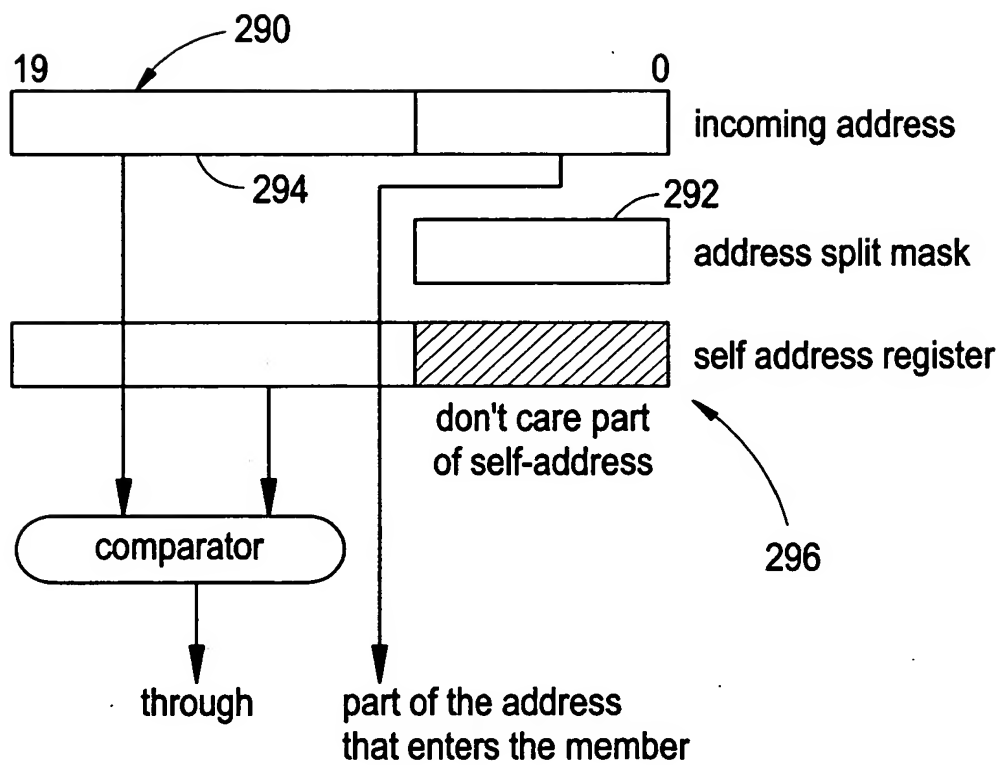


FIG. 29



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FIG. 30

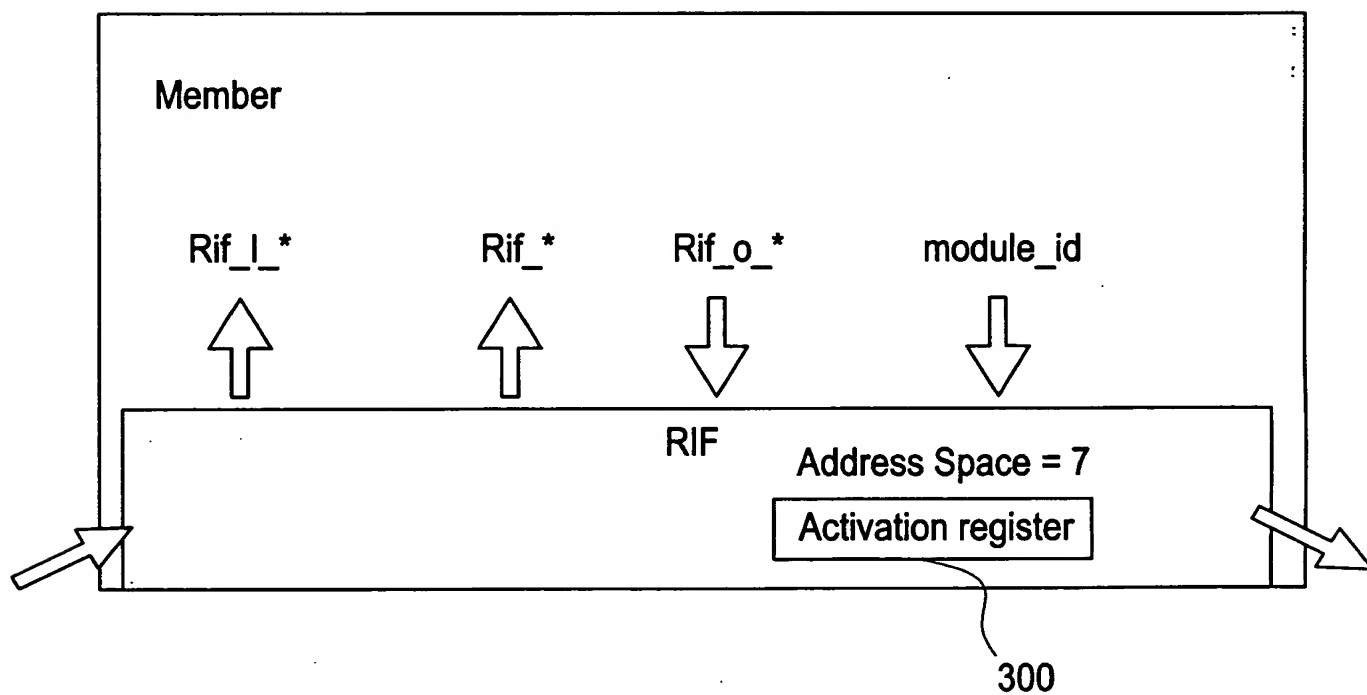
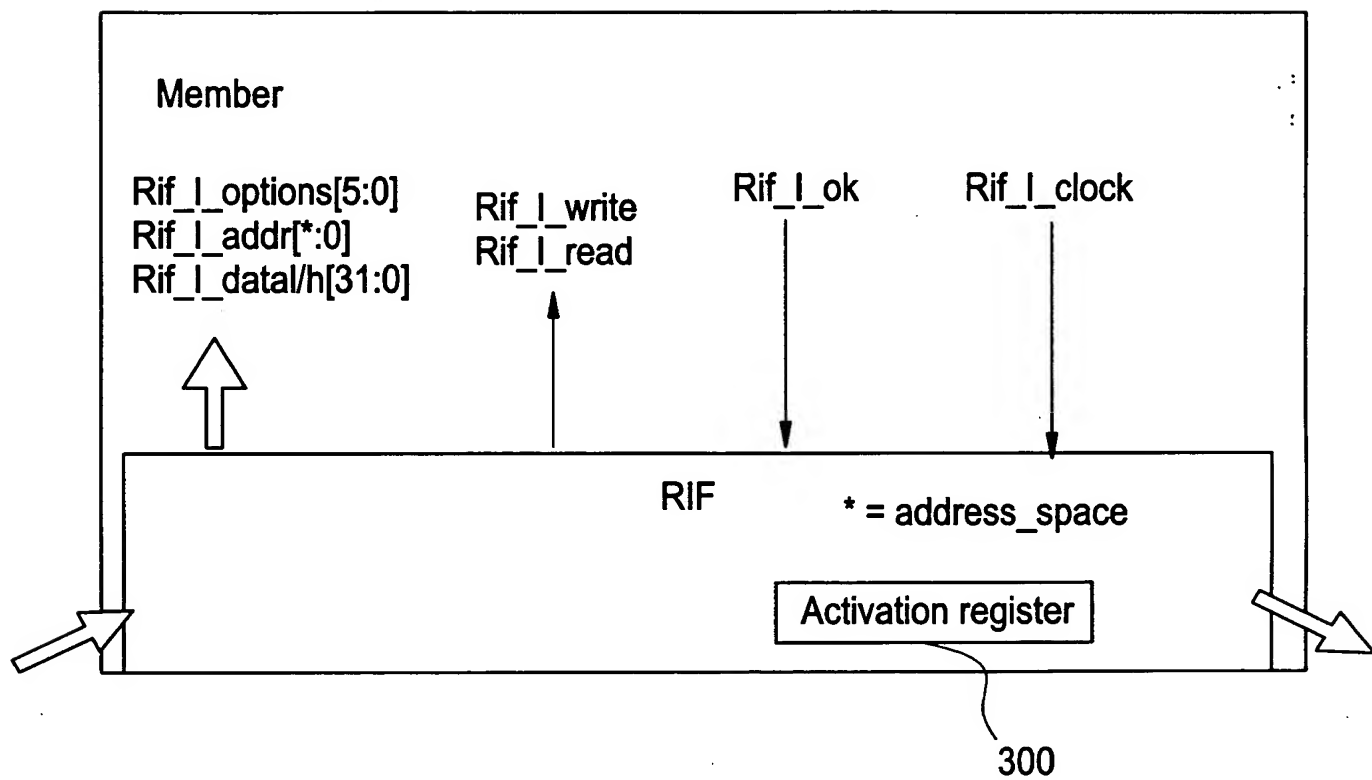
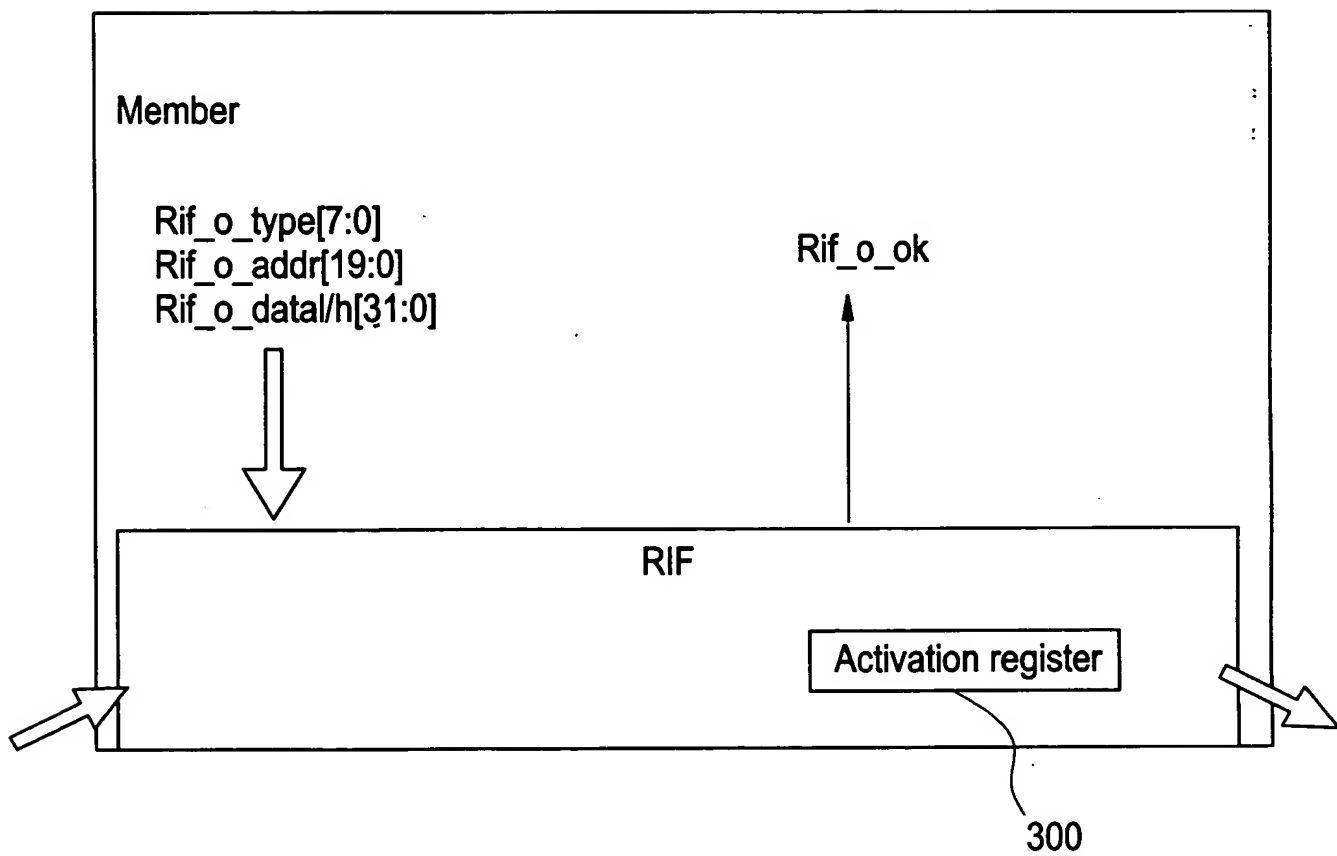


FIG. 31



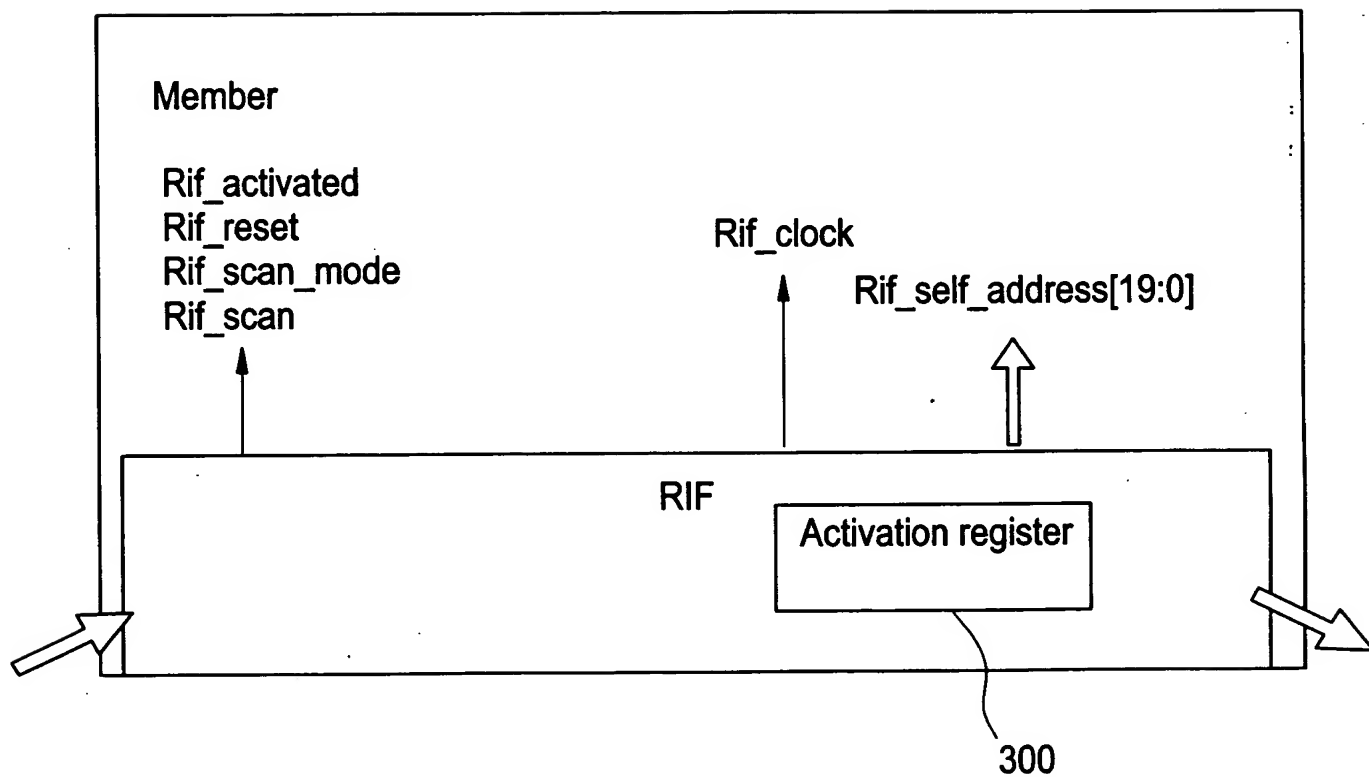
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FIG. 32



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FIG. 33



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FIG. 34

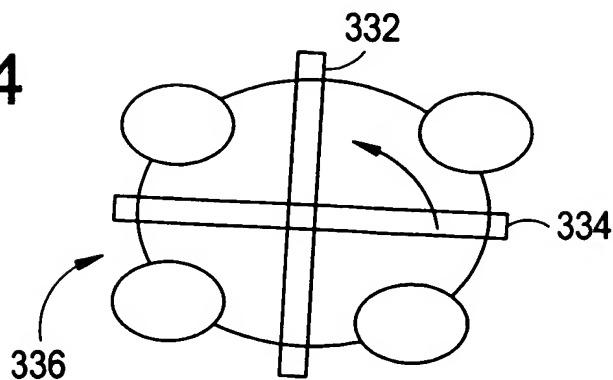


FIG. 35

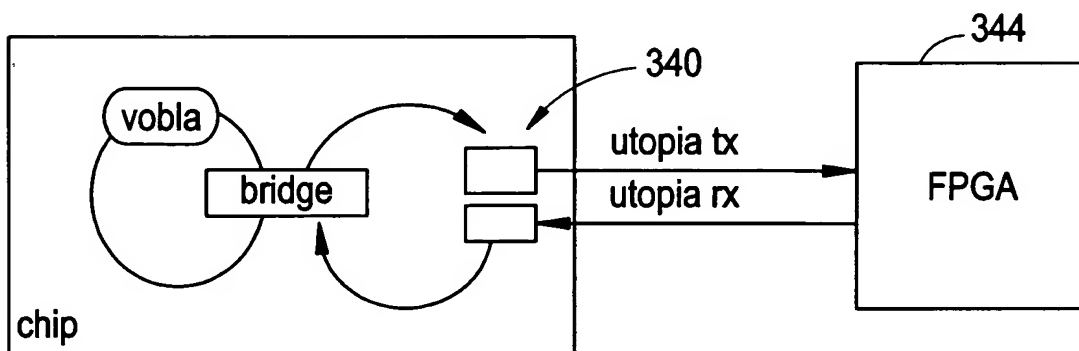
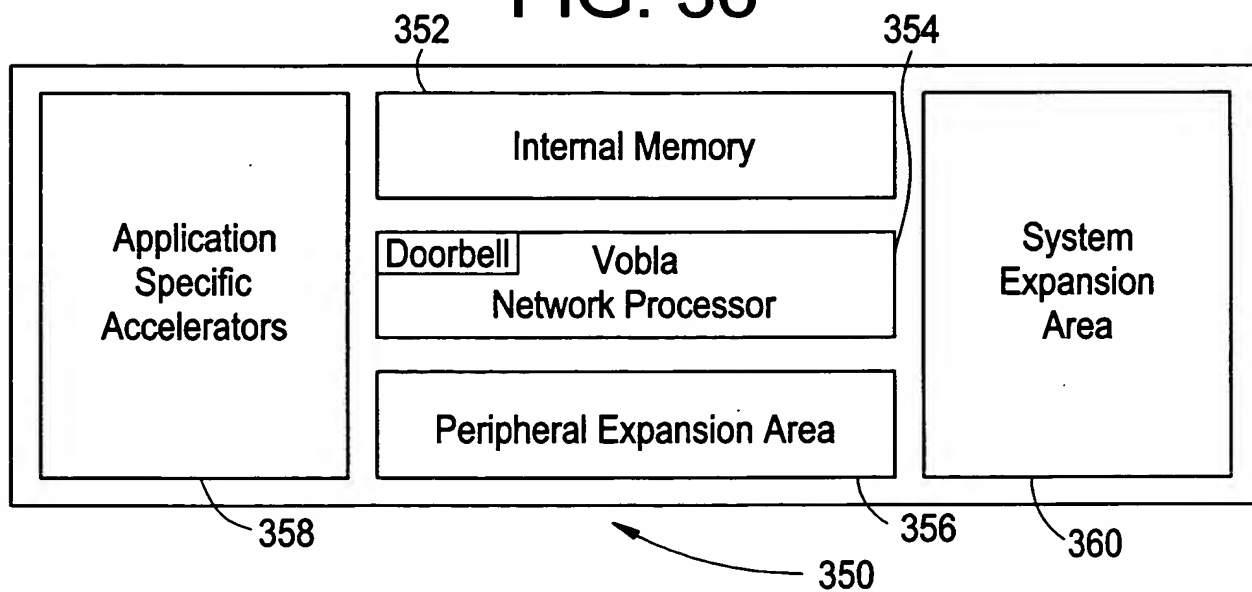


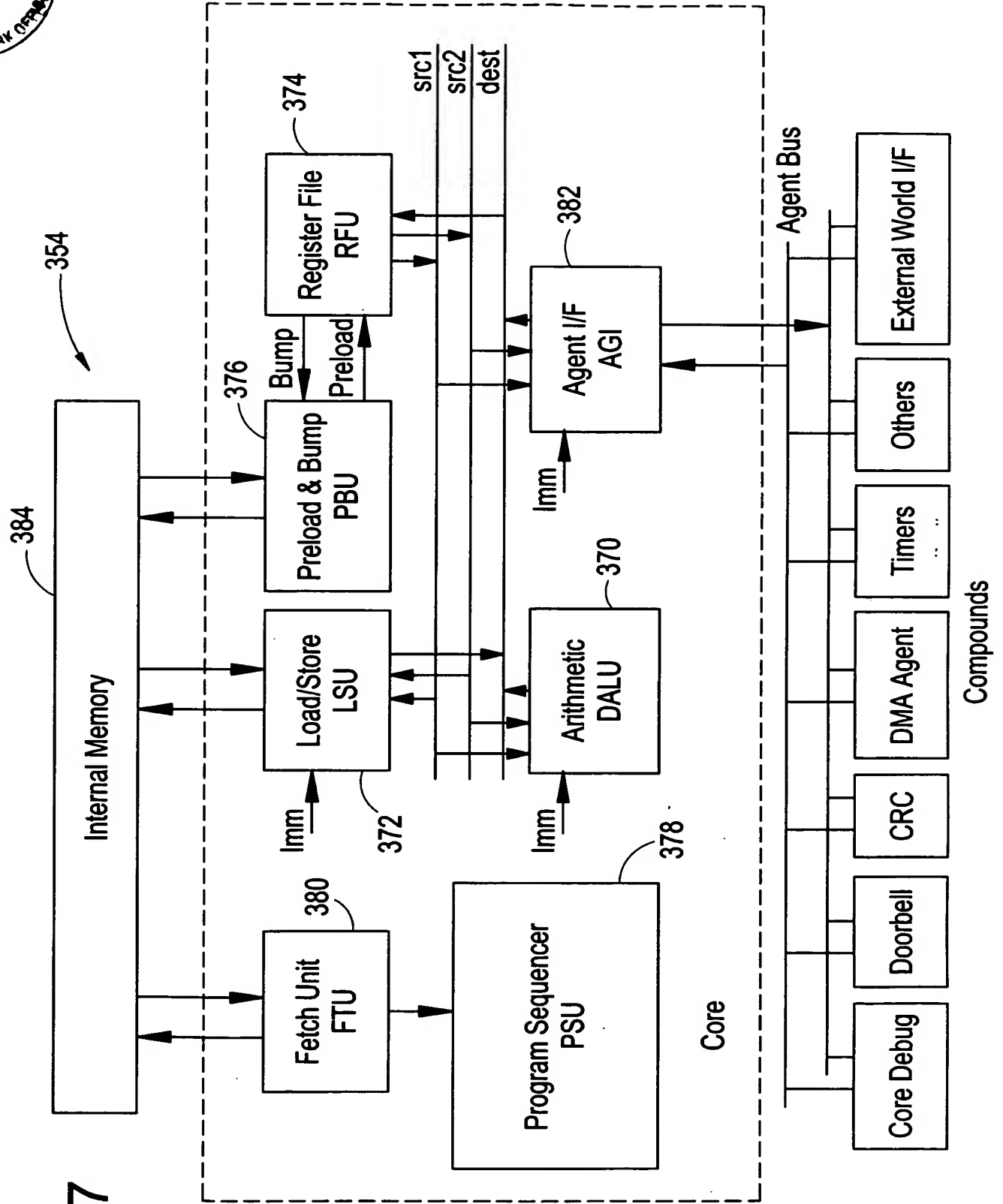
FIG. 36



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FIG. 37



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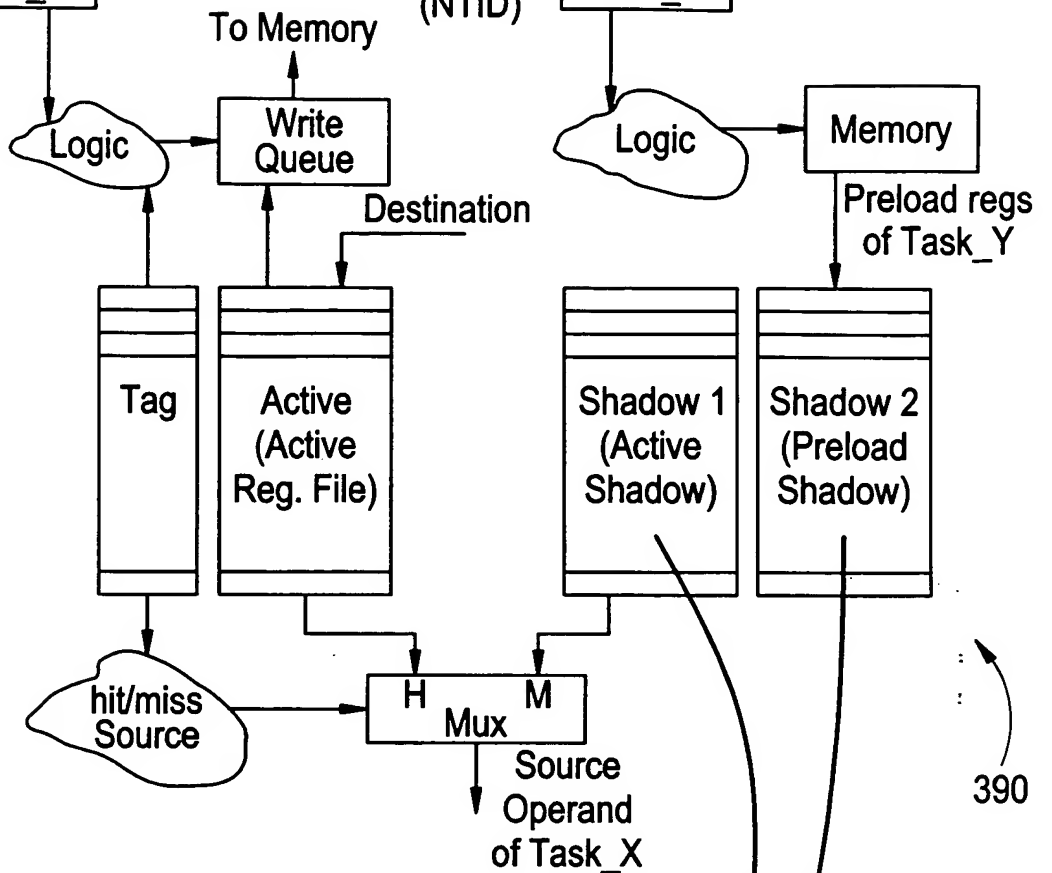
Current Task (CTID)

Task\_X

Next Task (NTID)

Task\_Y

TRADE MARK



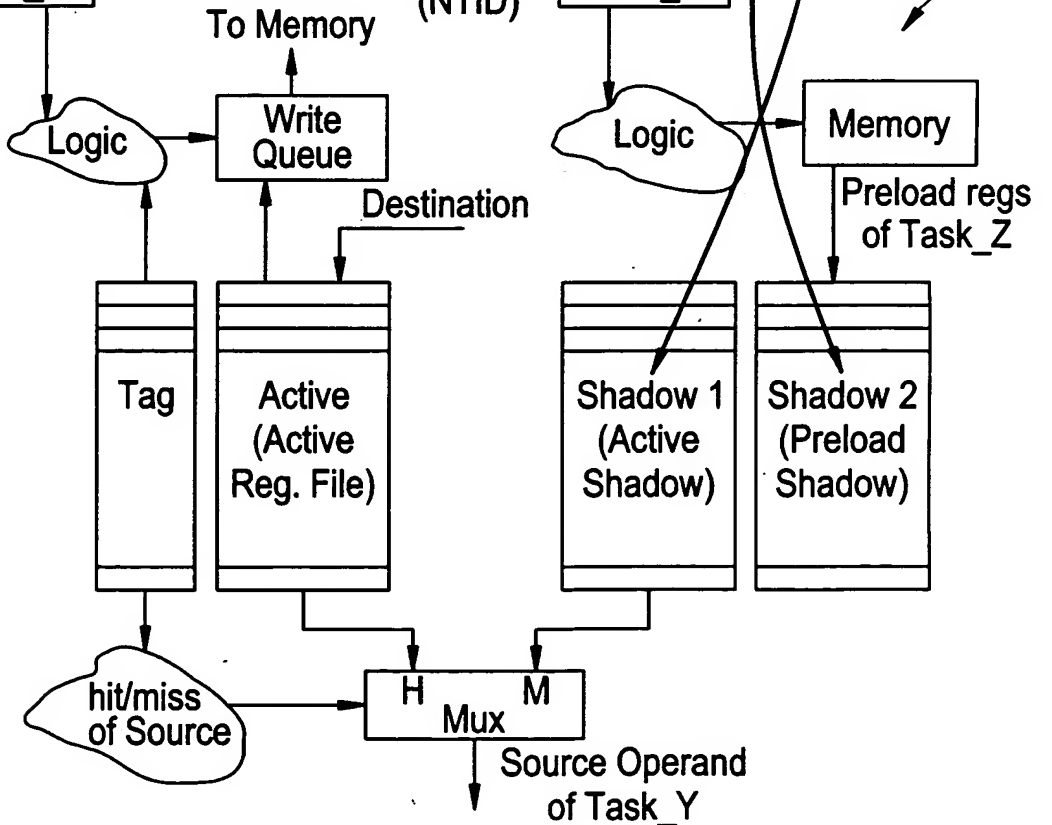
After a task switch

Current Task (CTID)

Task\_Y

Next Task (NTID)

Task\_Z



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FIG. 39

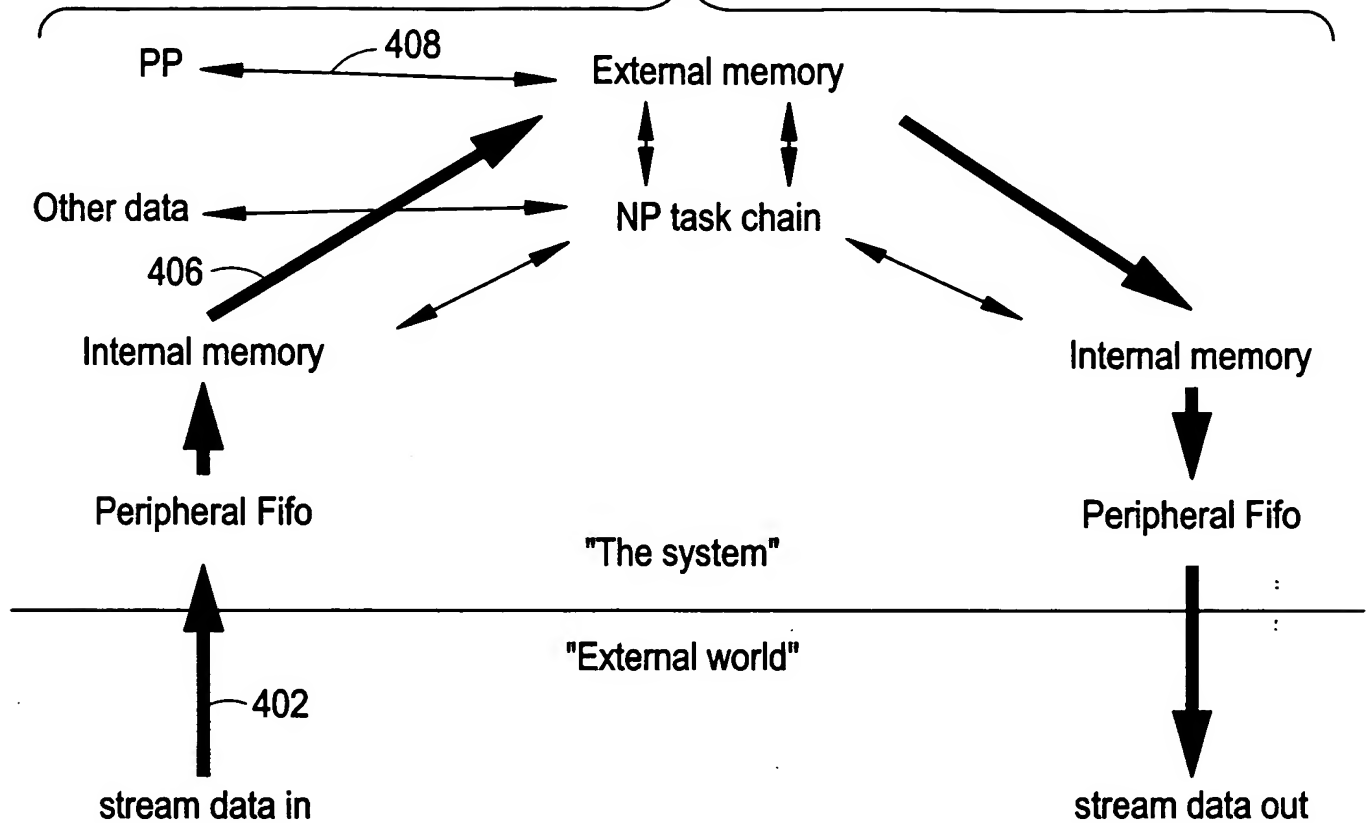
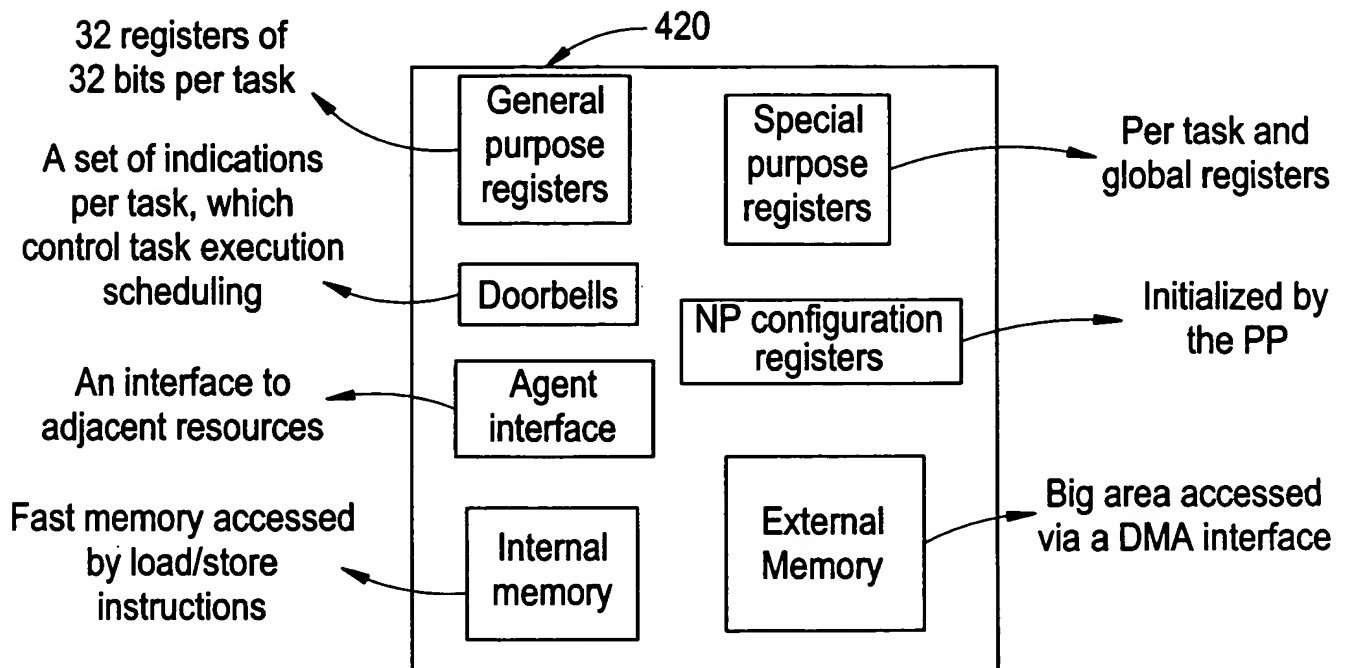


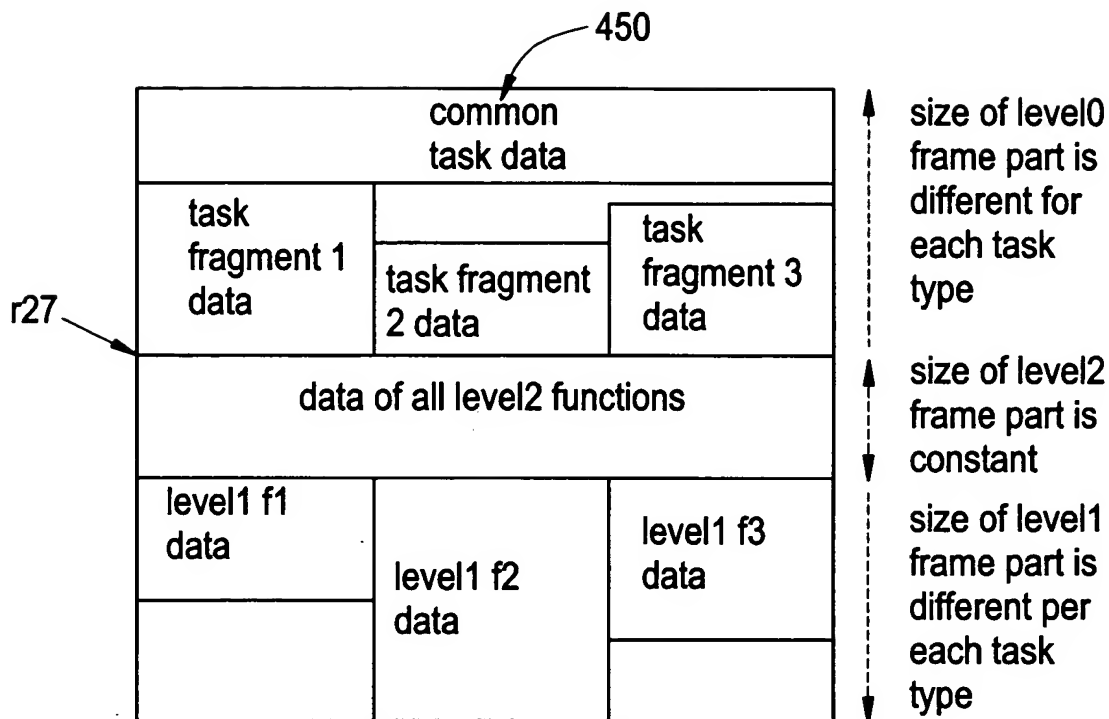
FIG. 40



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FIG. 43



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FIG. 44

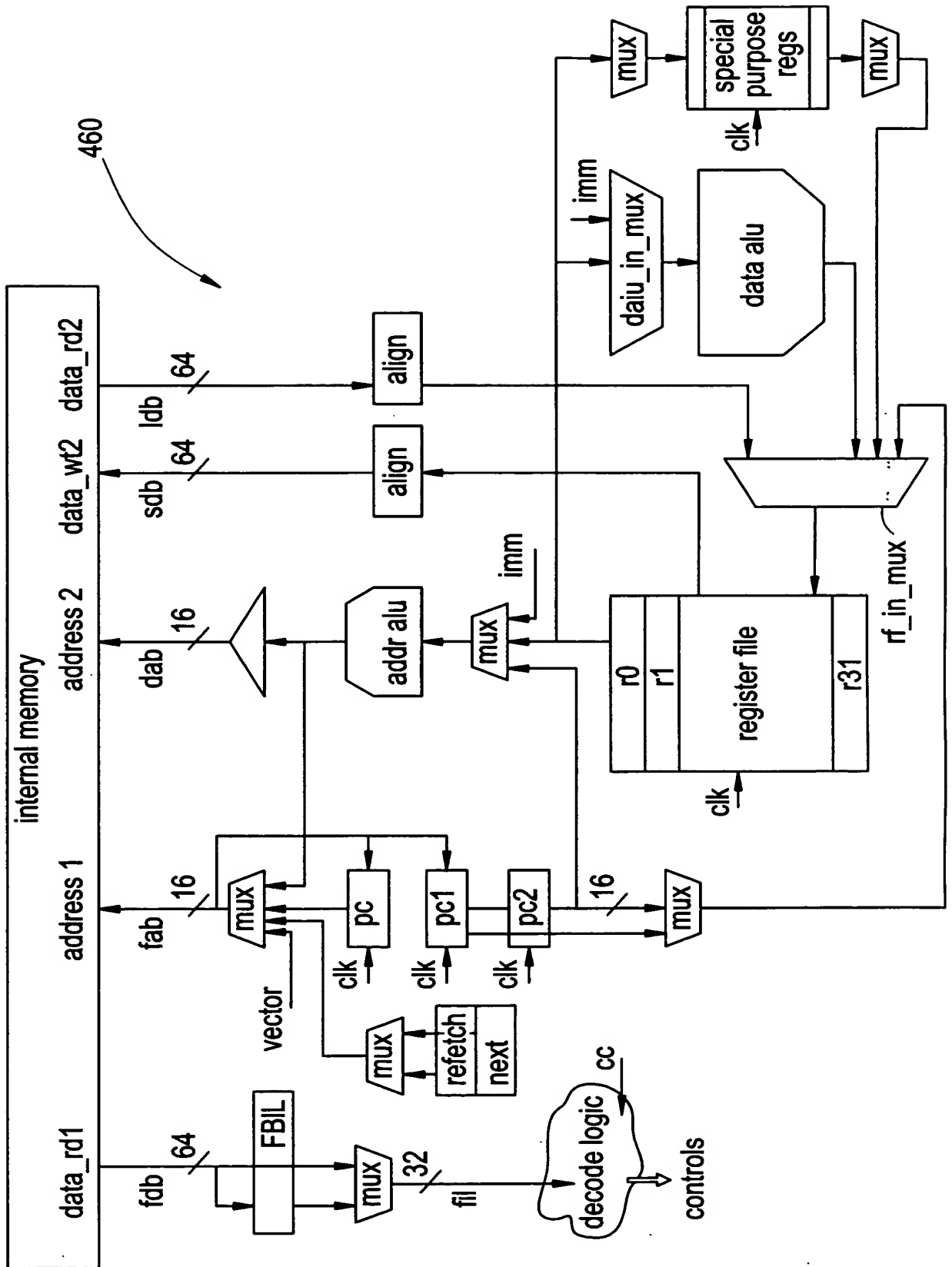
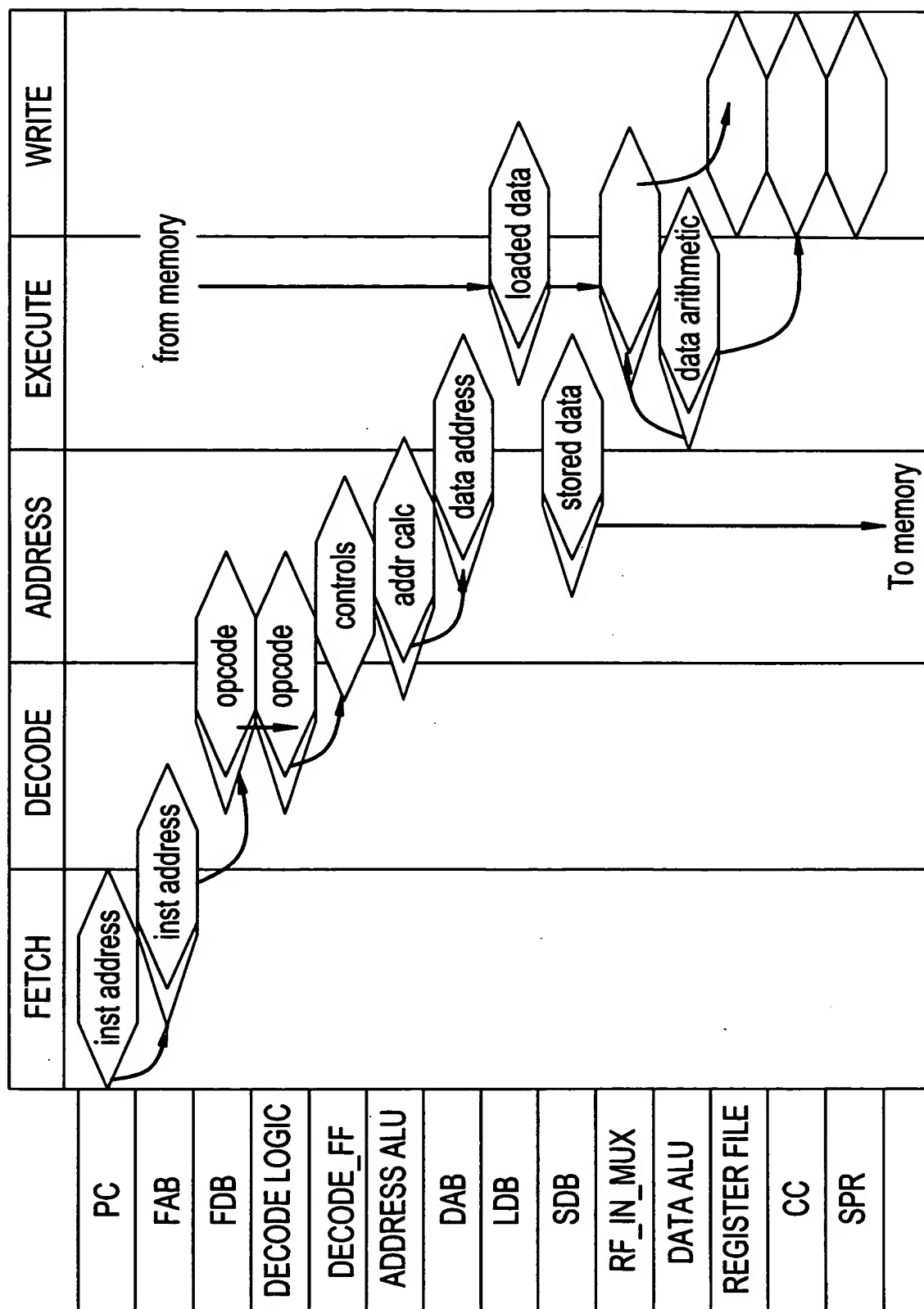


FIG. 45



## - Flip Flop

## - Logic



FIG. 46

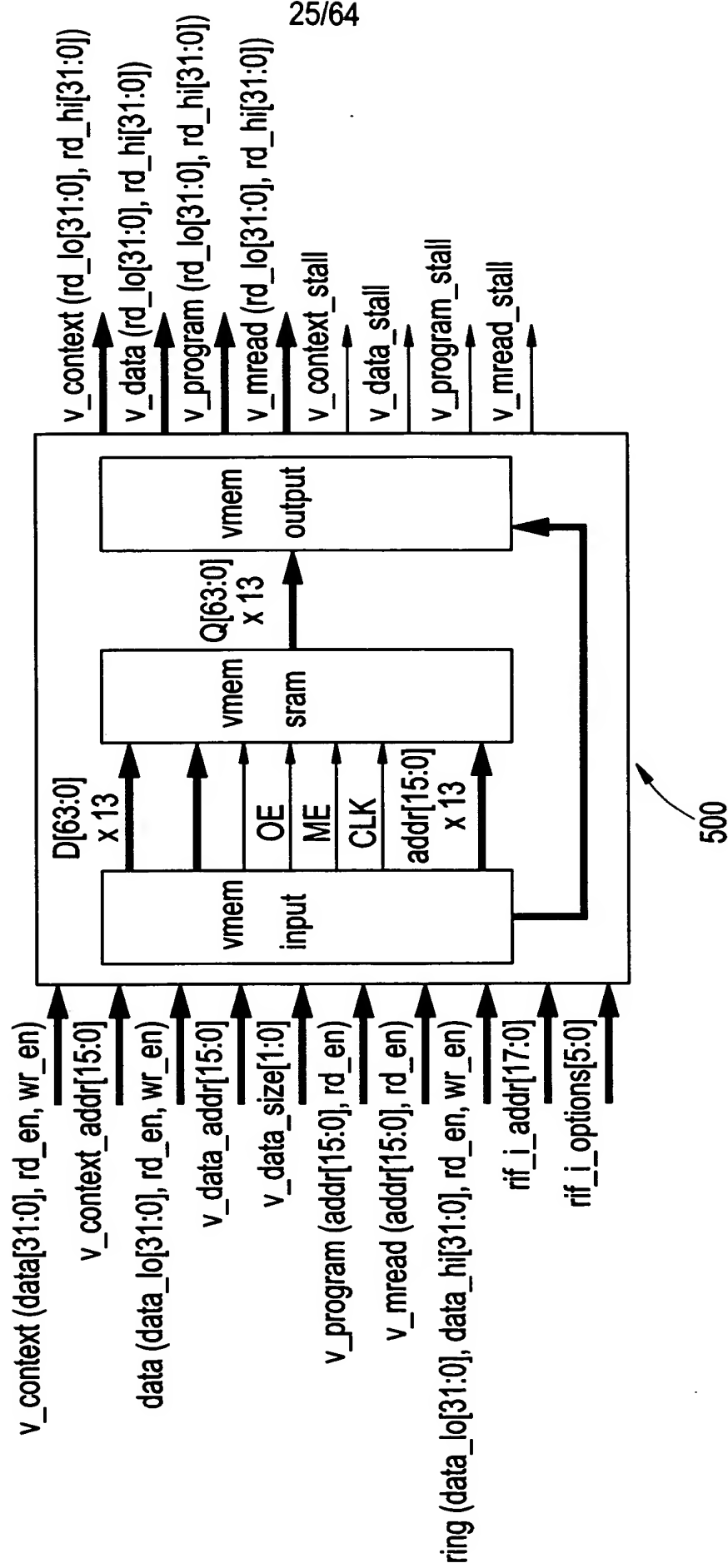
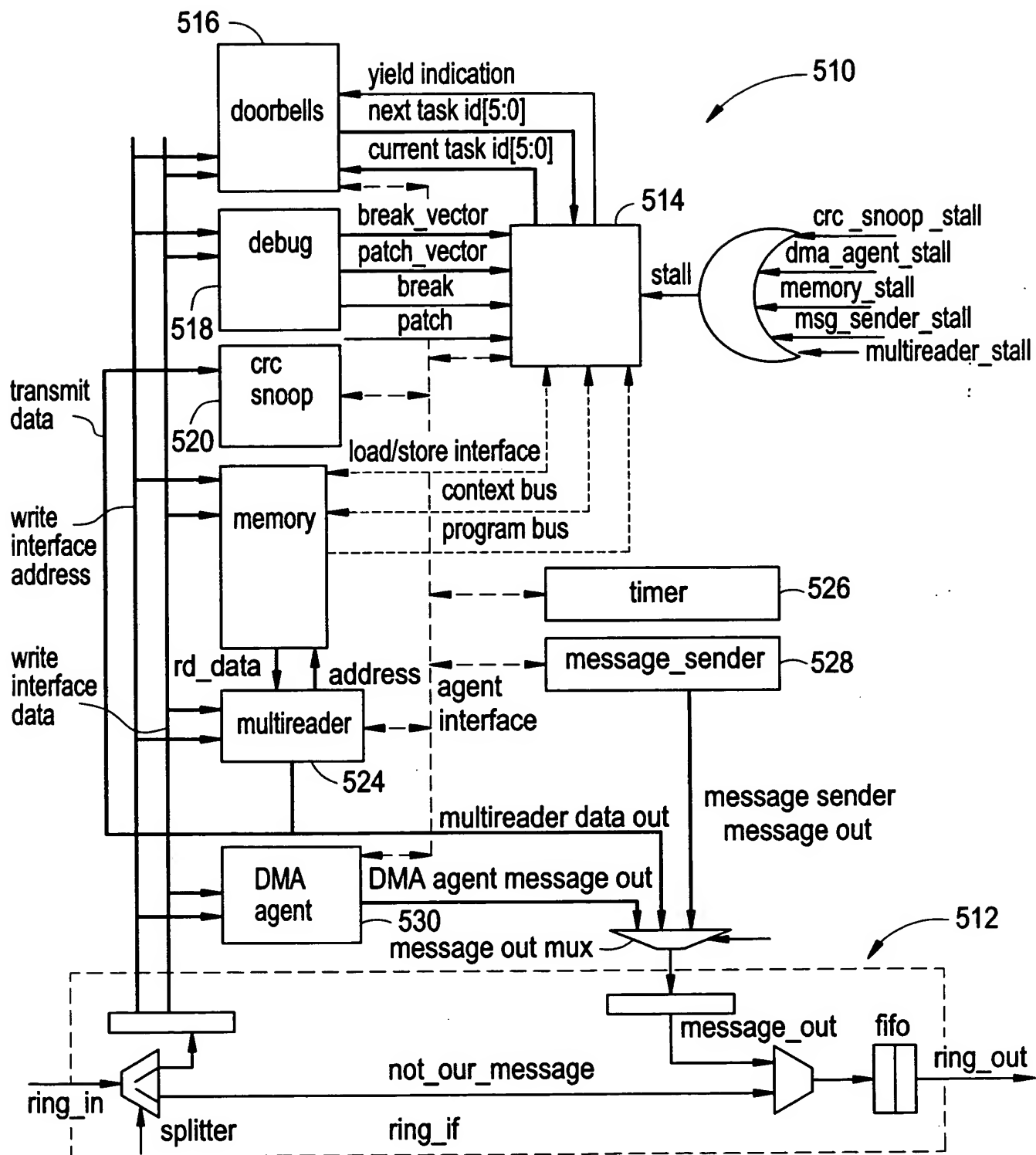


FIG. 47



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FIG. 48

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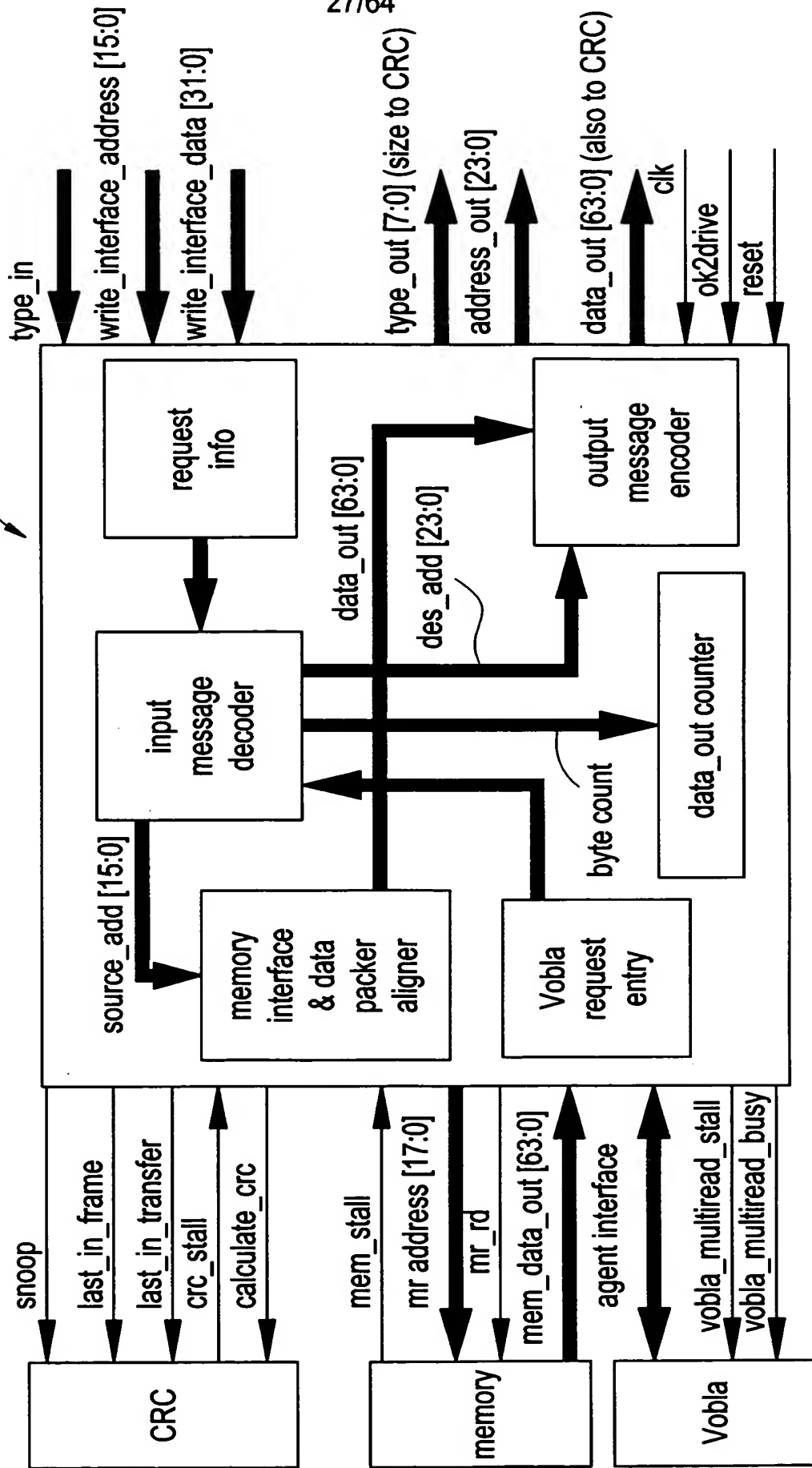


FIG. 49

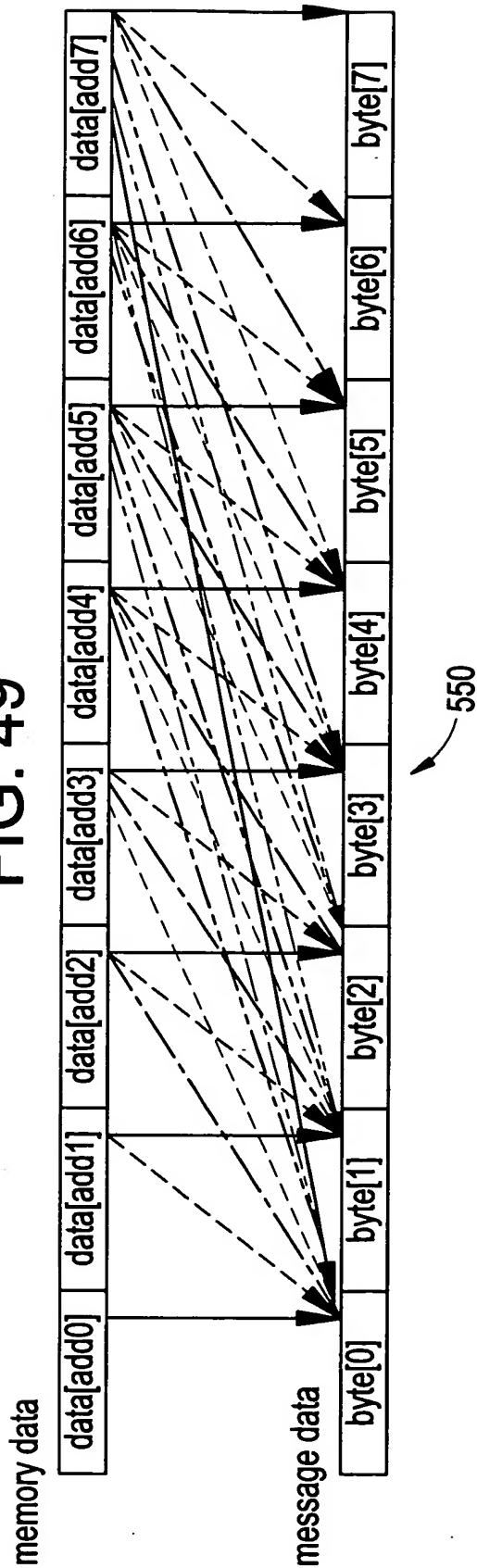


FIG. 50

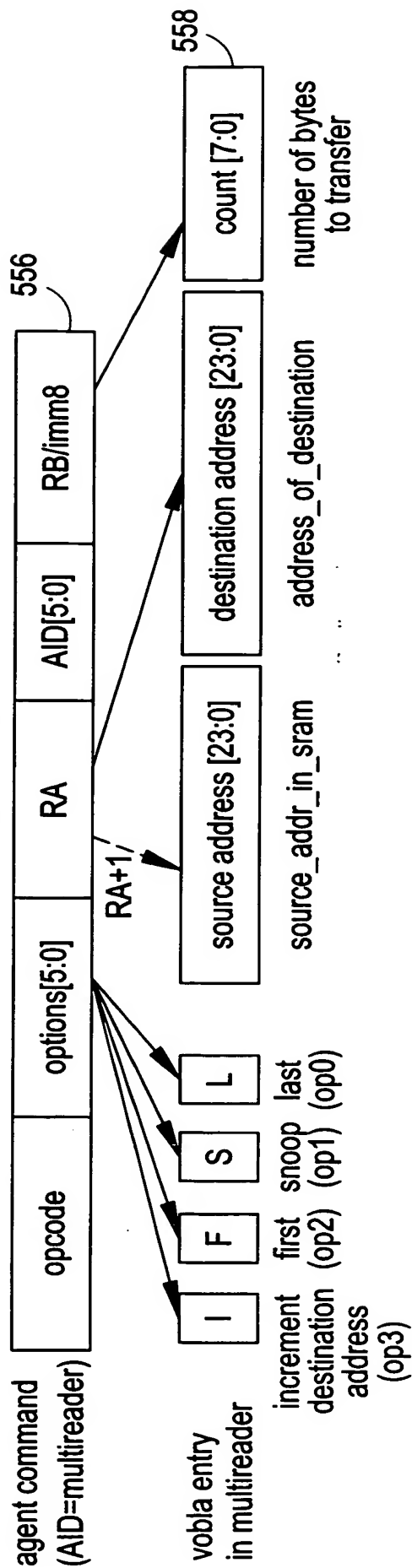


FIG. 51

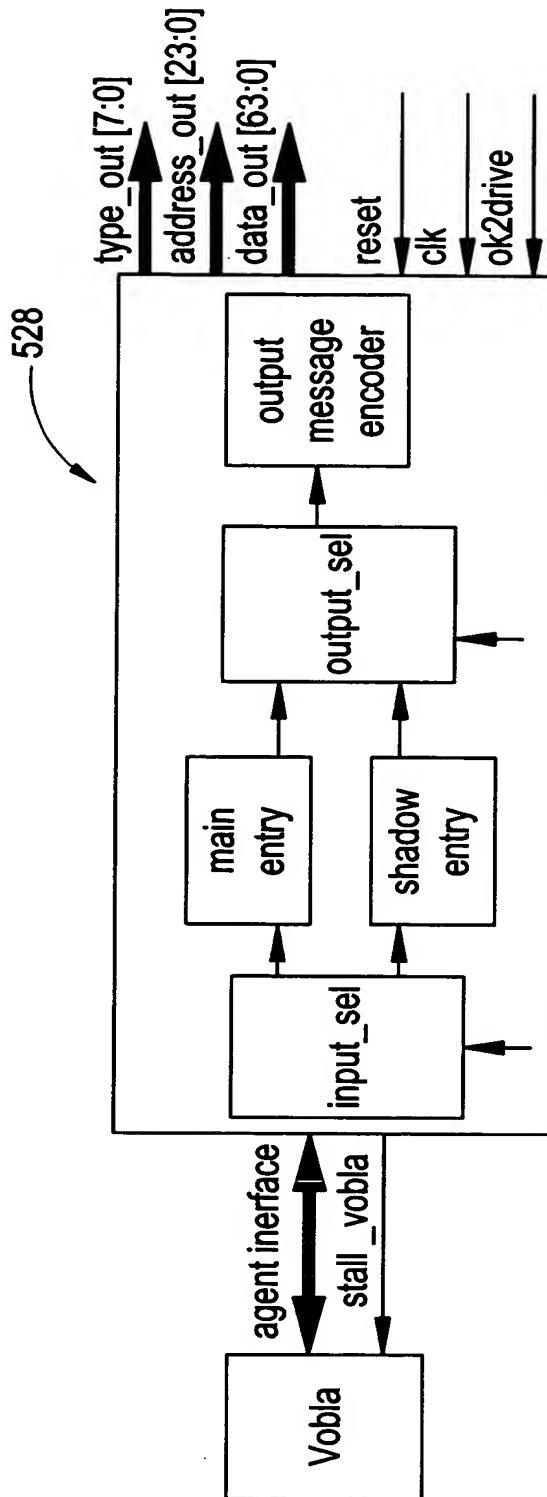


FIG. 52

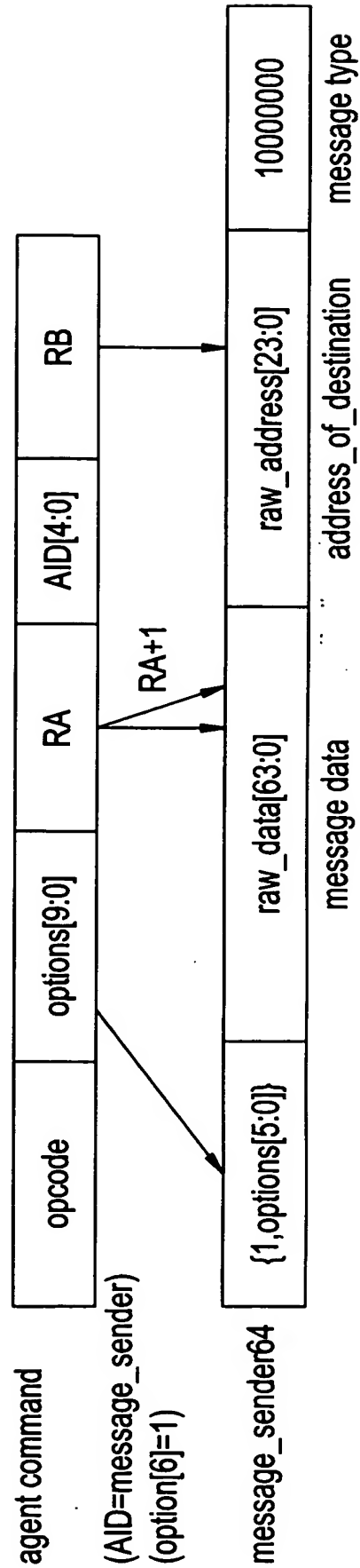
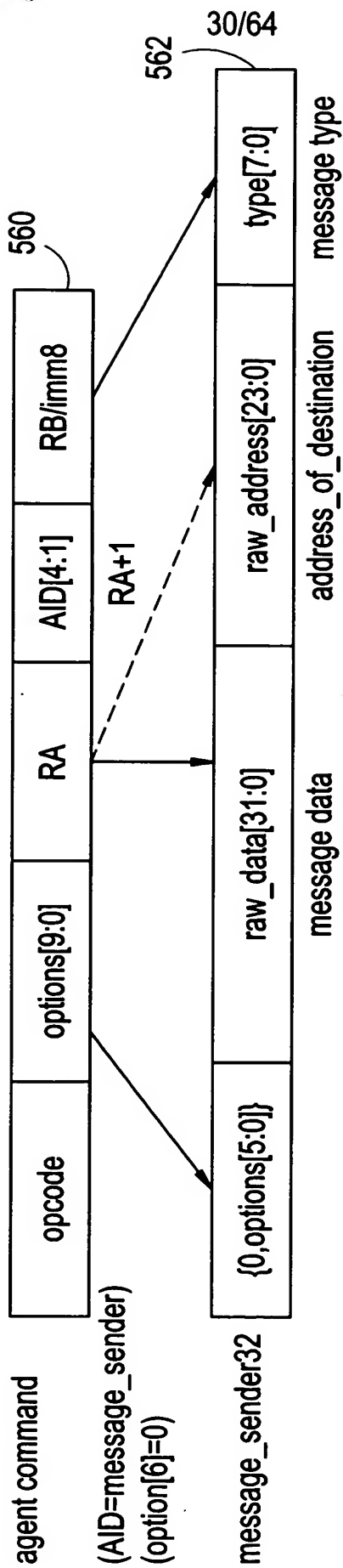


FIG. 53

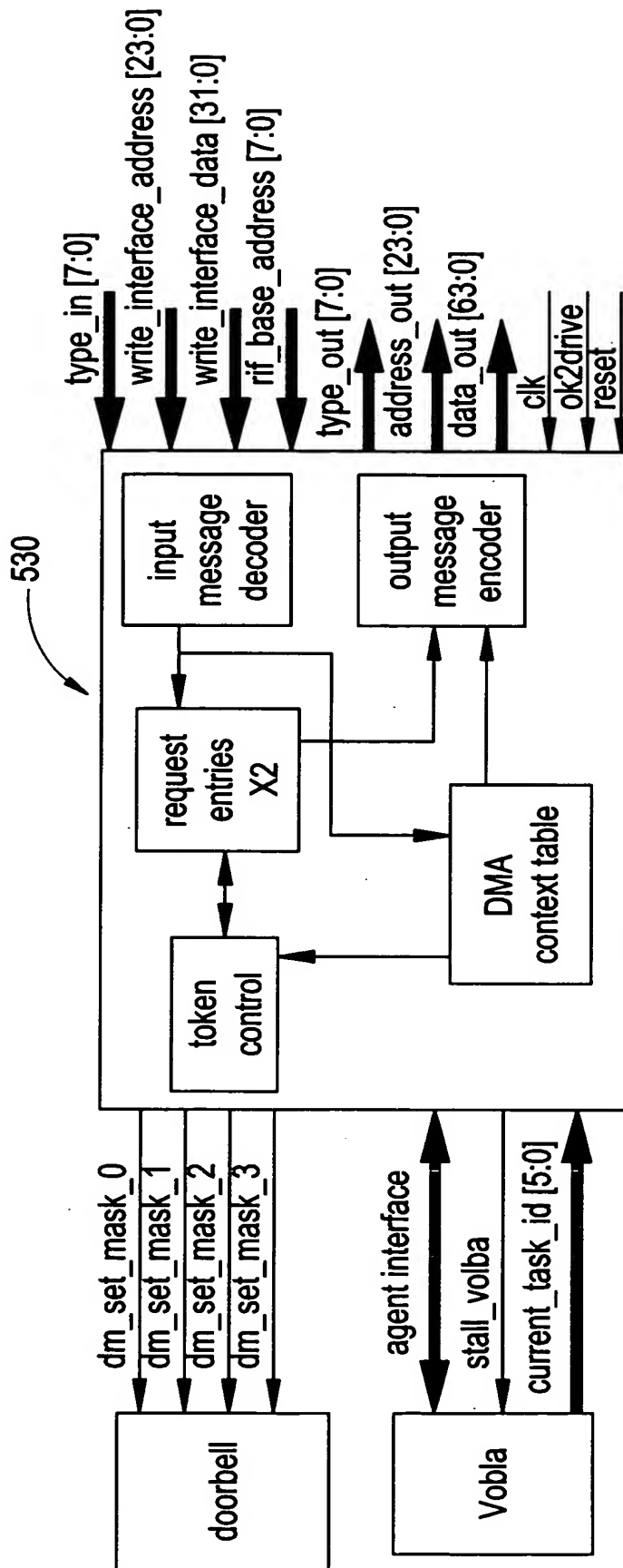


FIG. 54

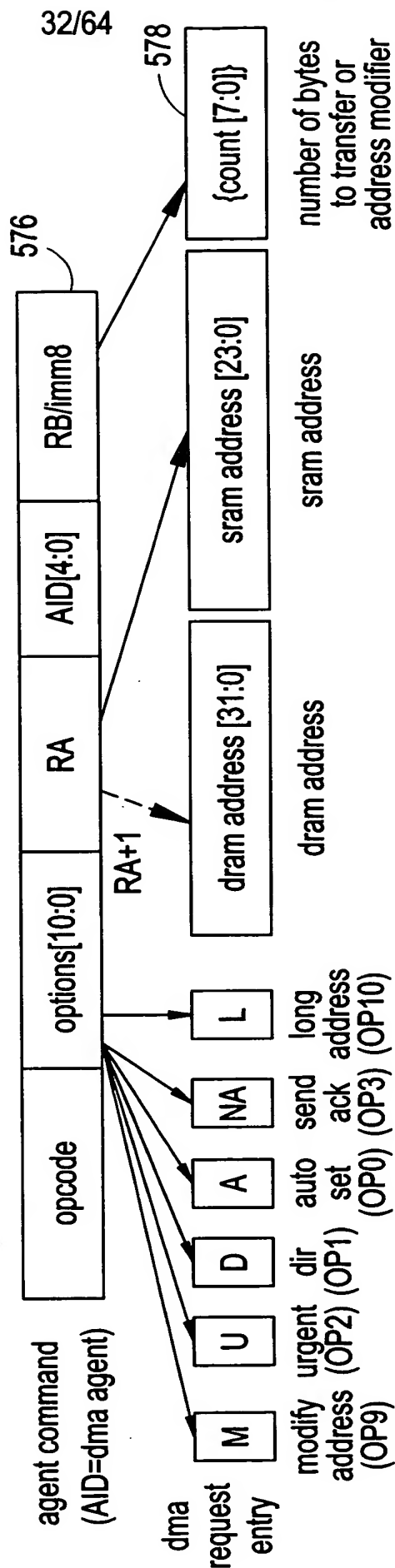




FIG. 55

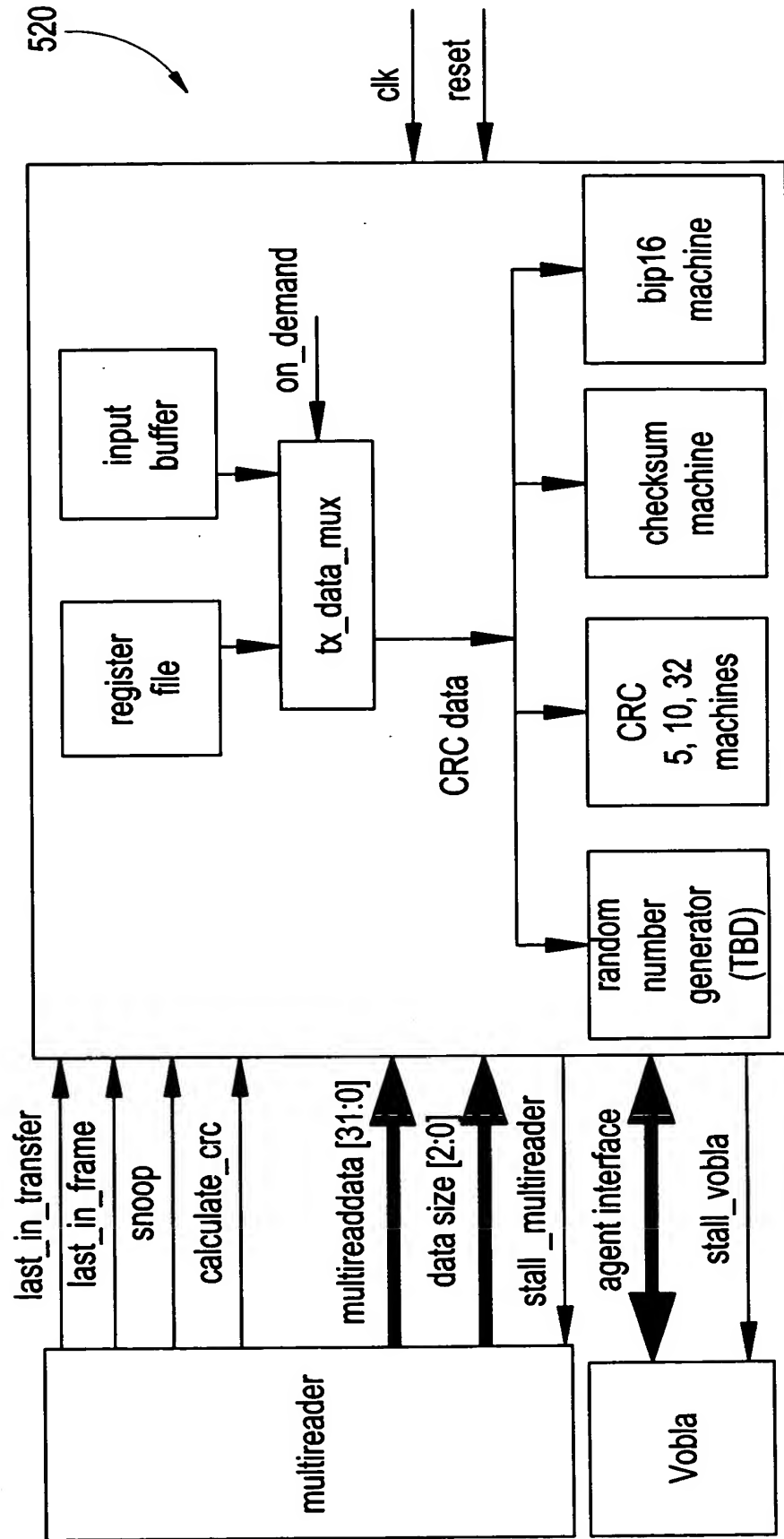




FIG. 56

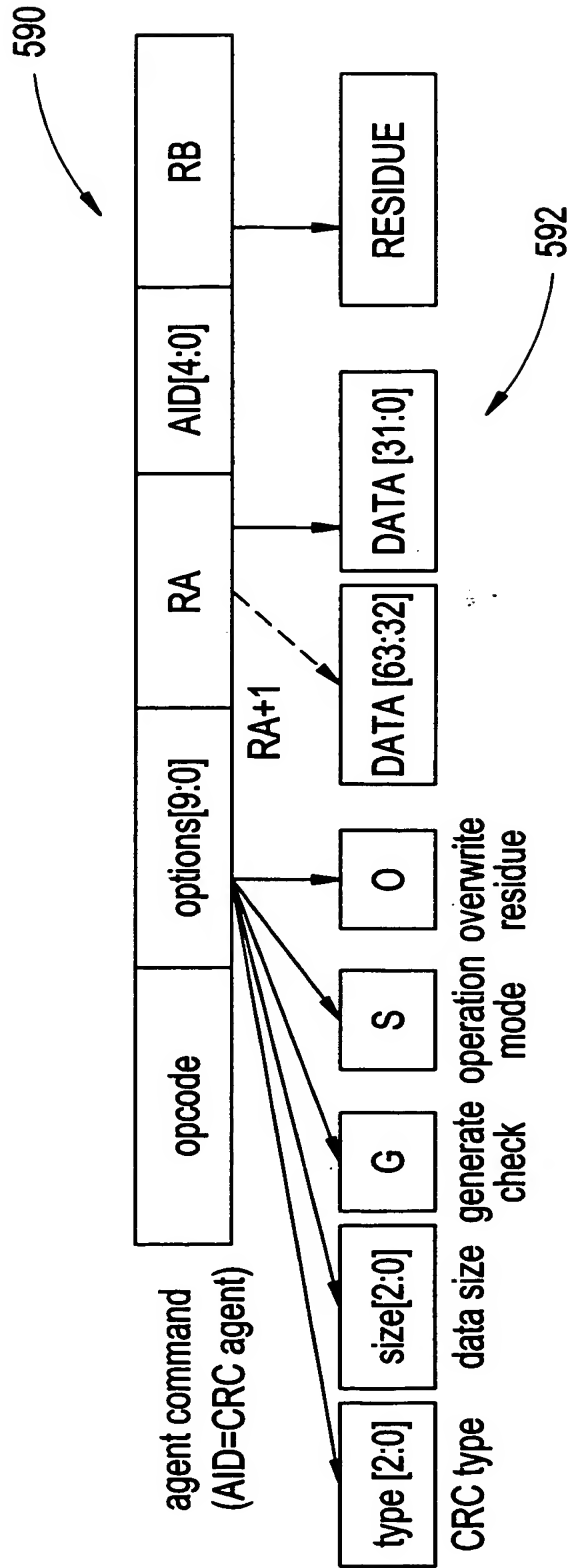


FIG. 57

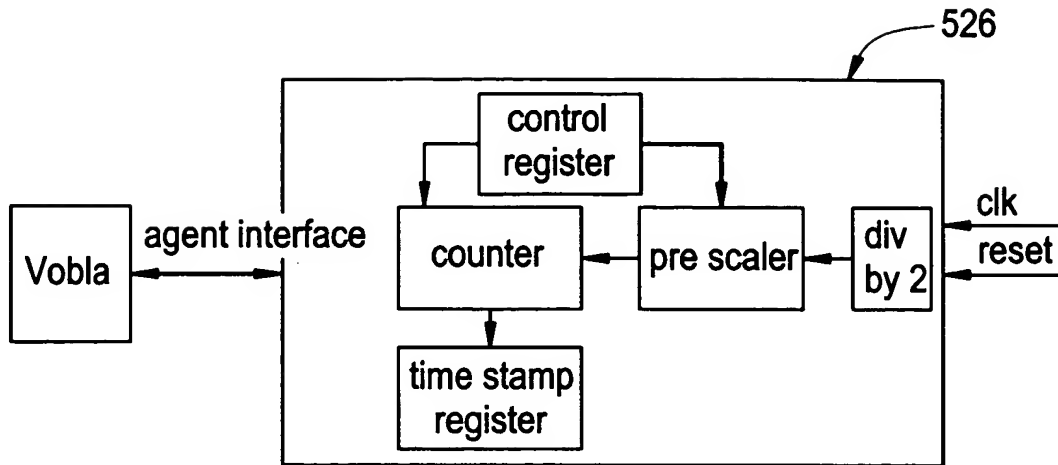


FIG. 58

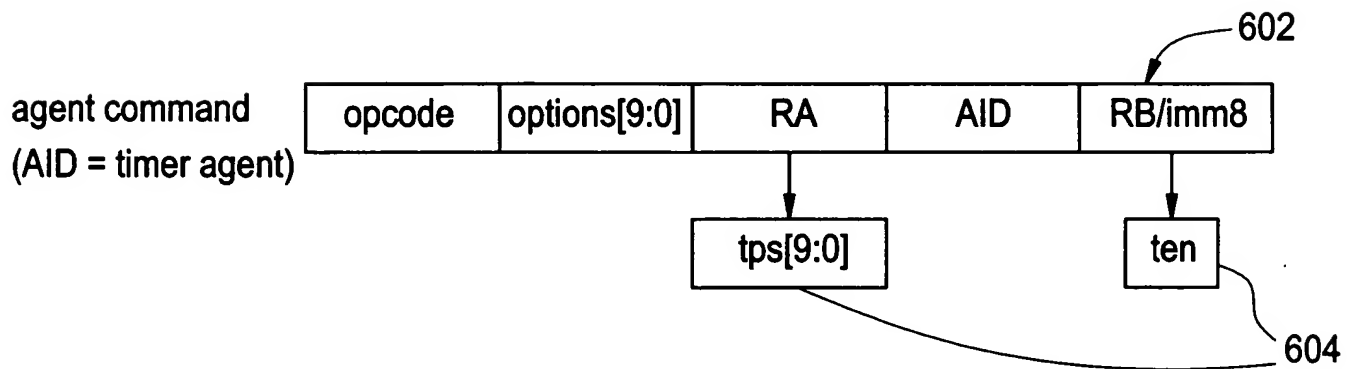




FIG. 61

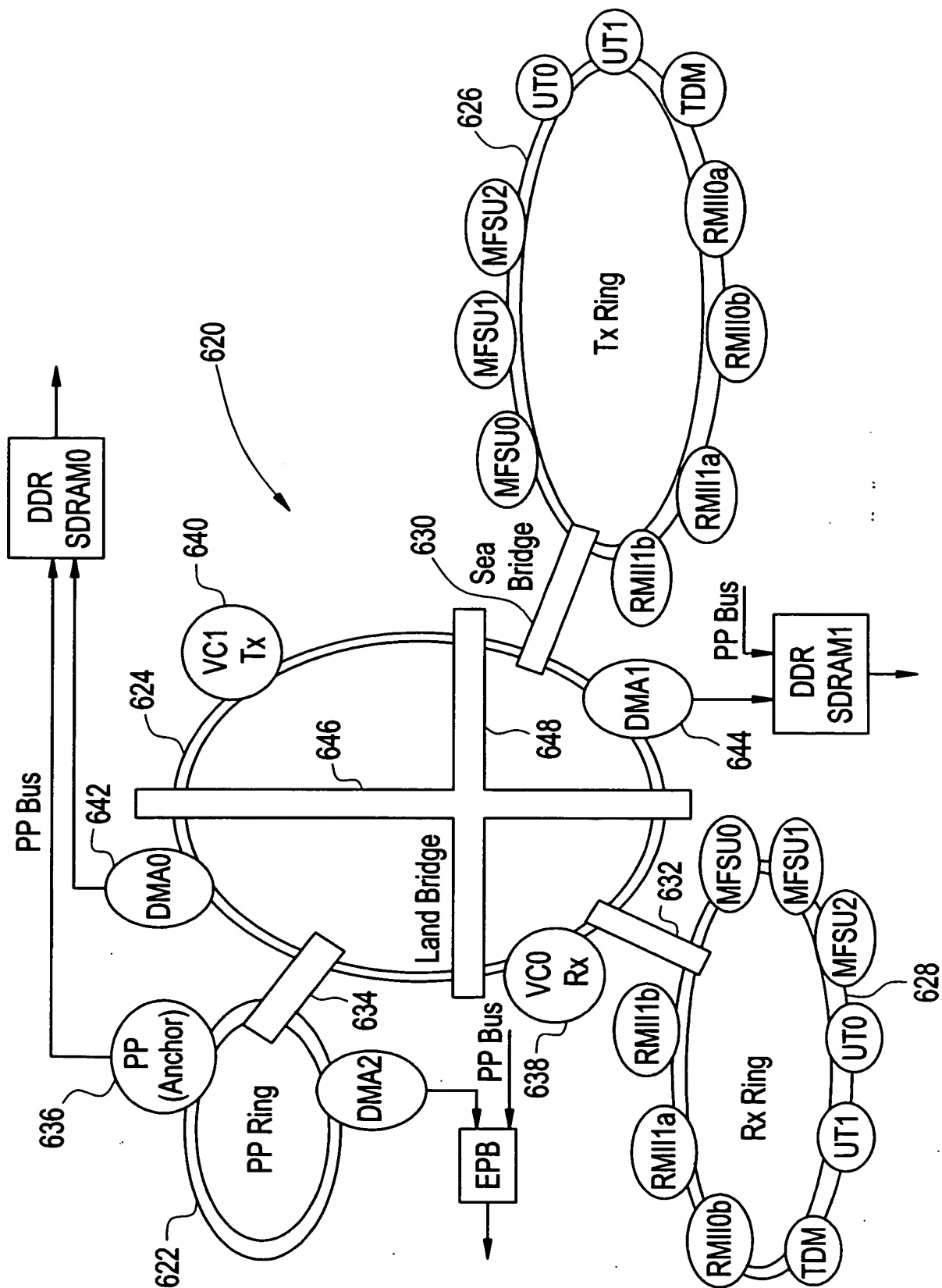


FIG. 62

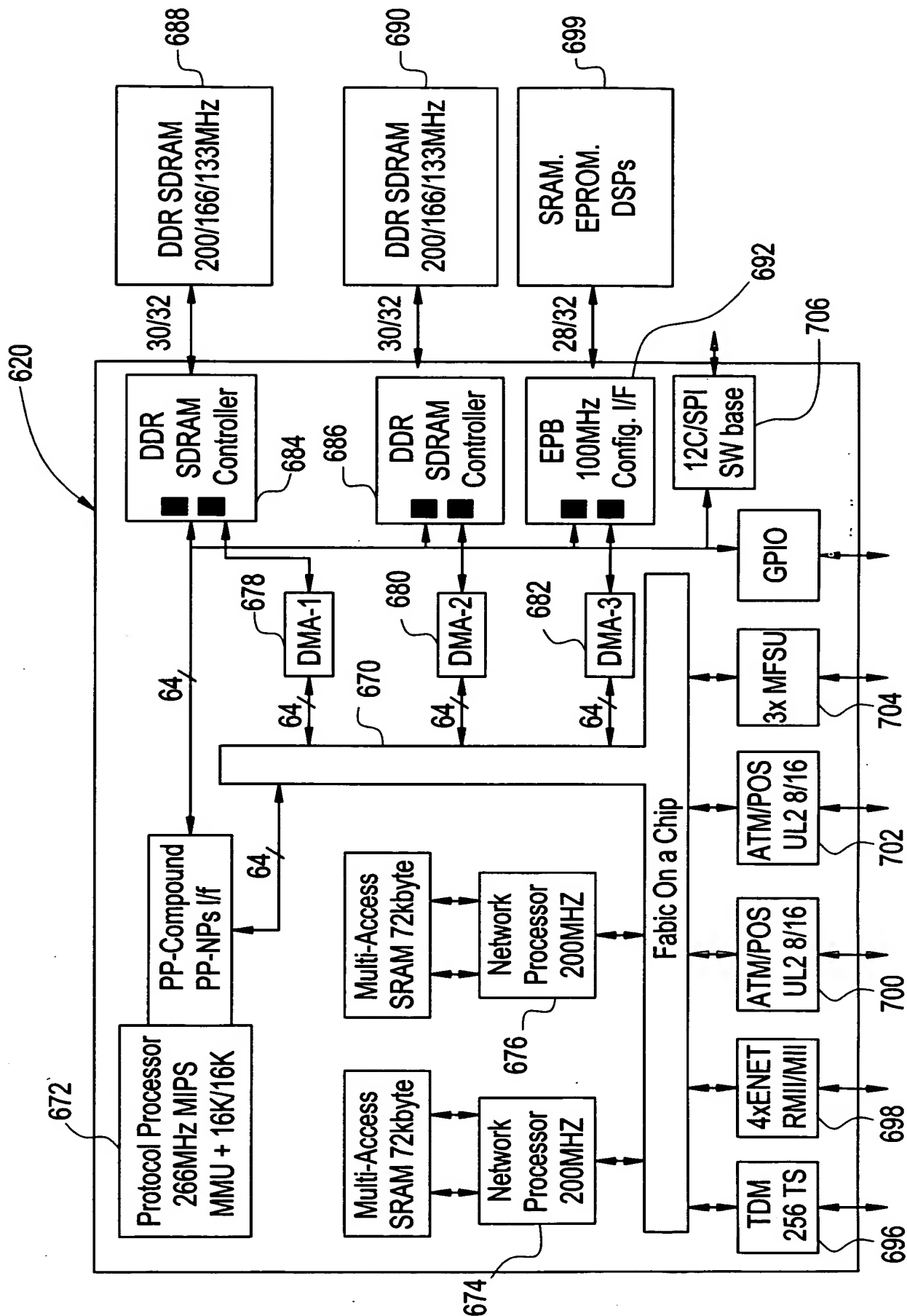
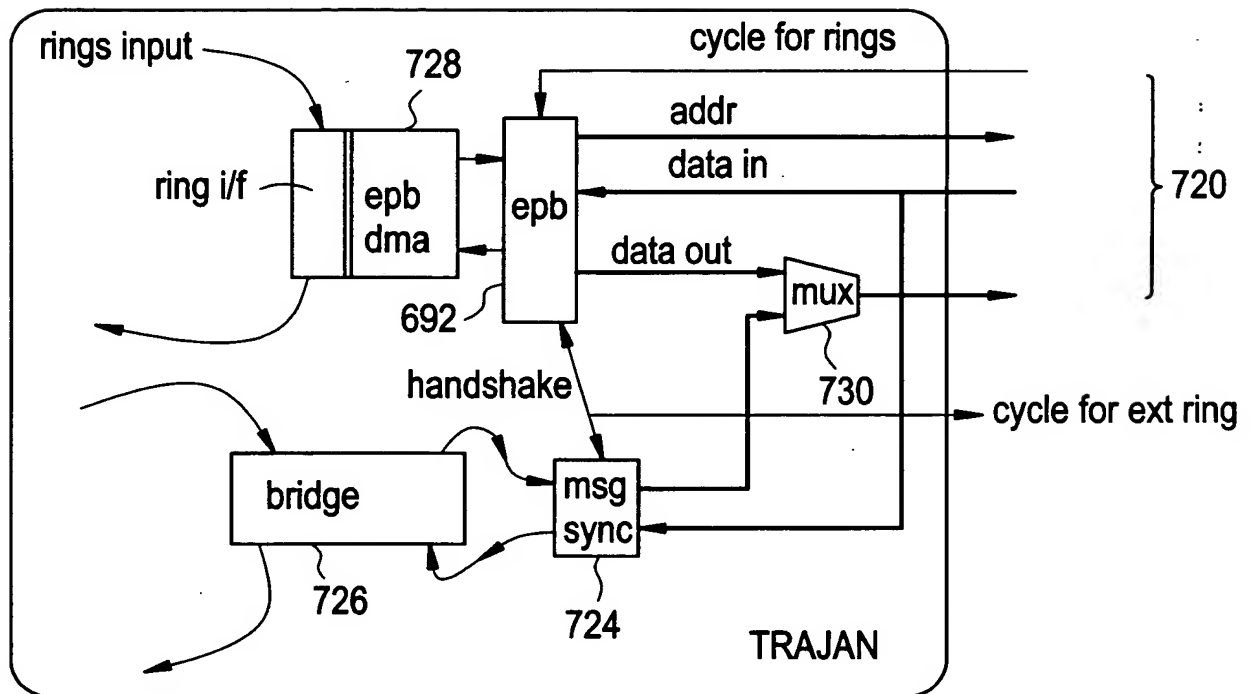
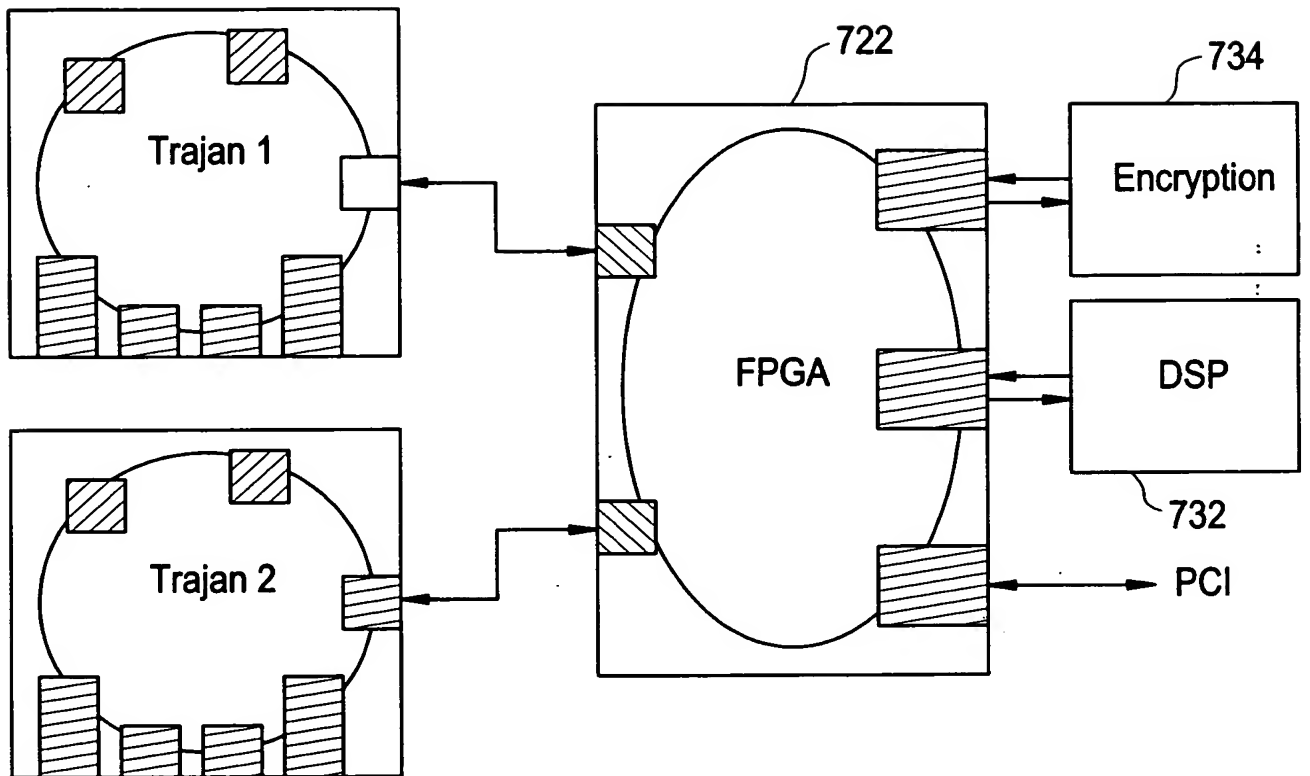





FIG. 63



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FIG. 64



-  Processor
-  Functional unit
-  External ring interface

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FIG. 65

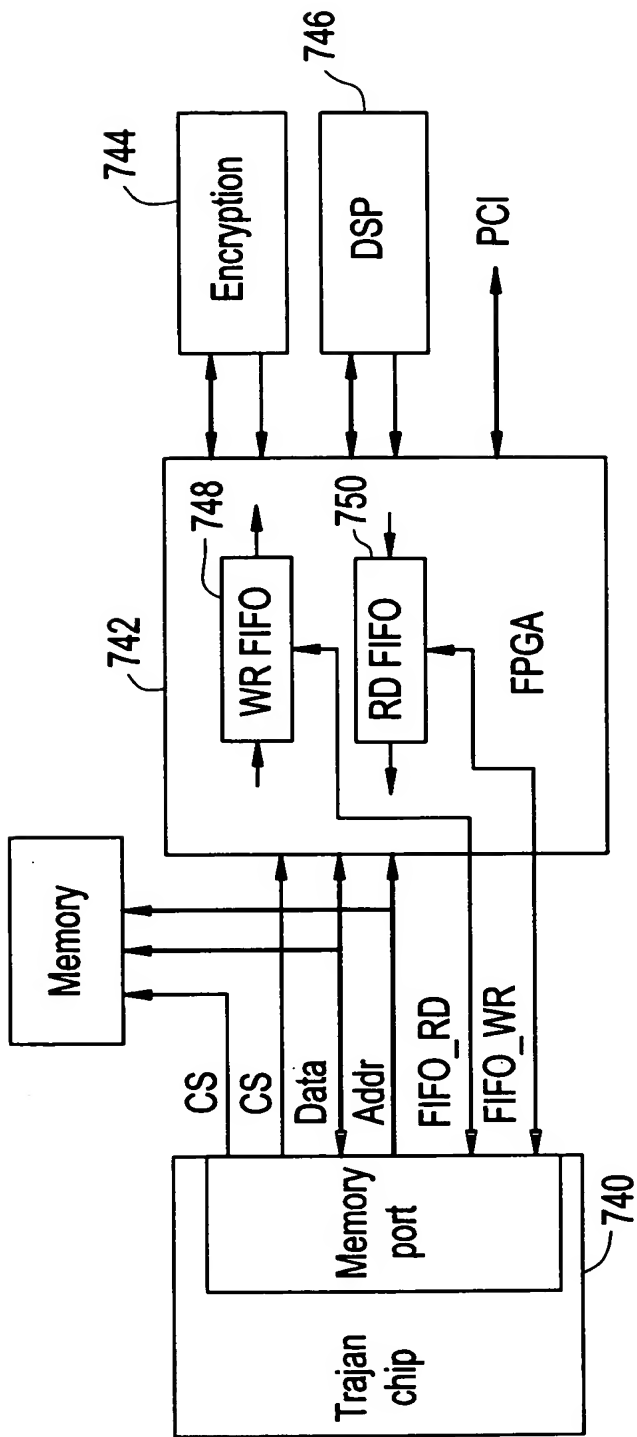




FIG. 66

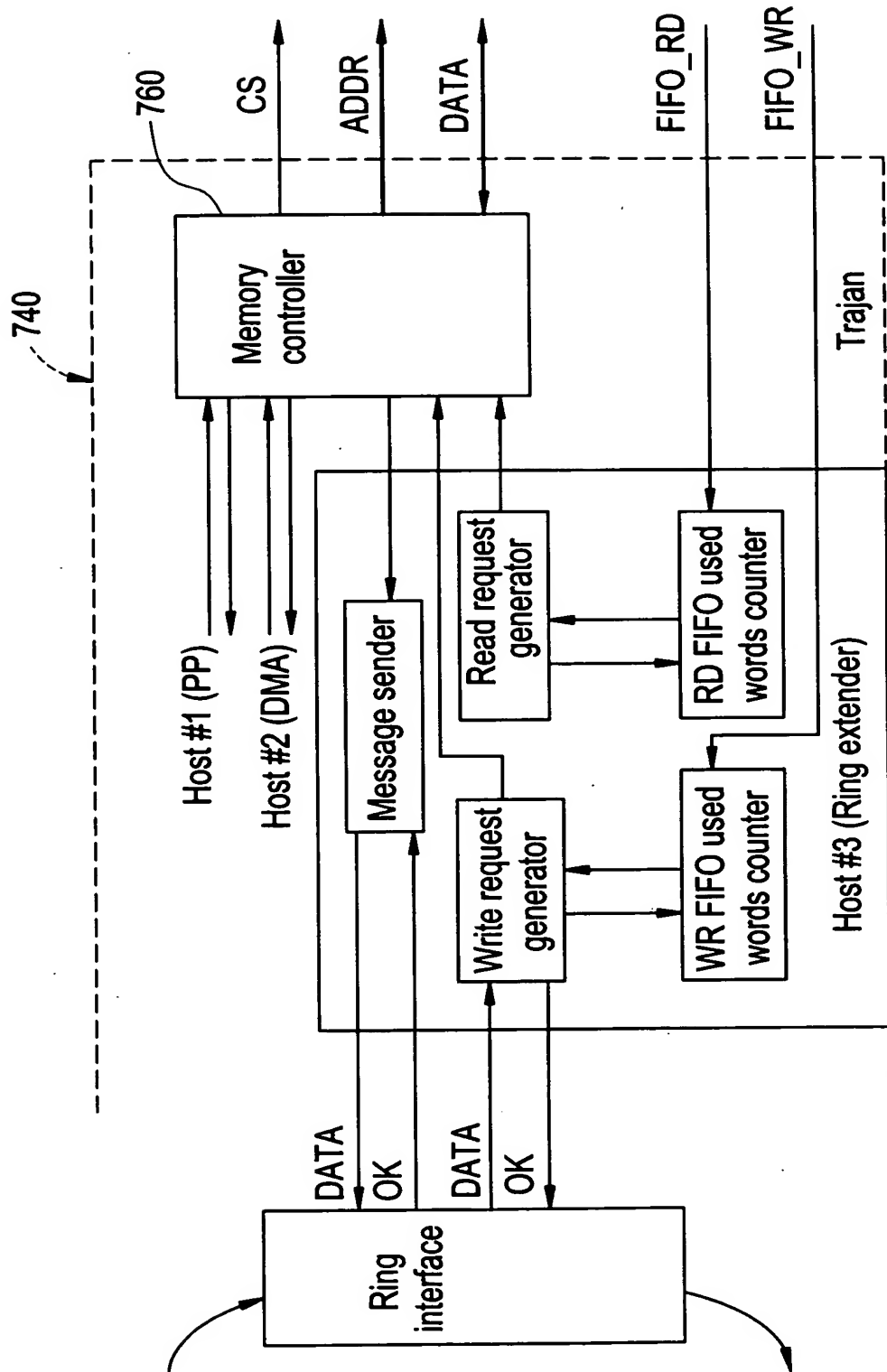


FIG. 67

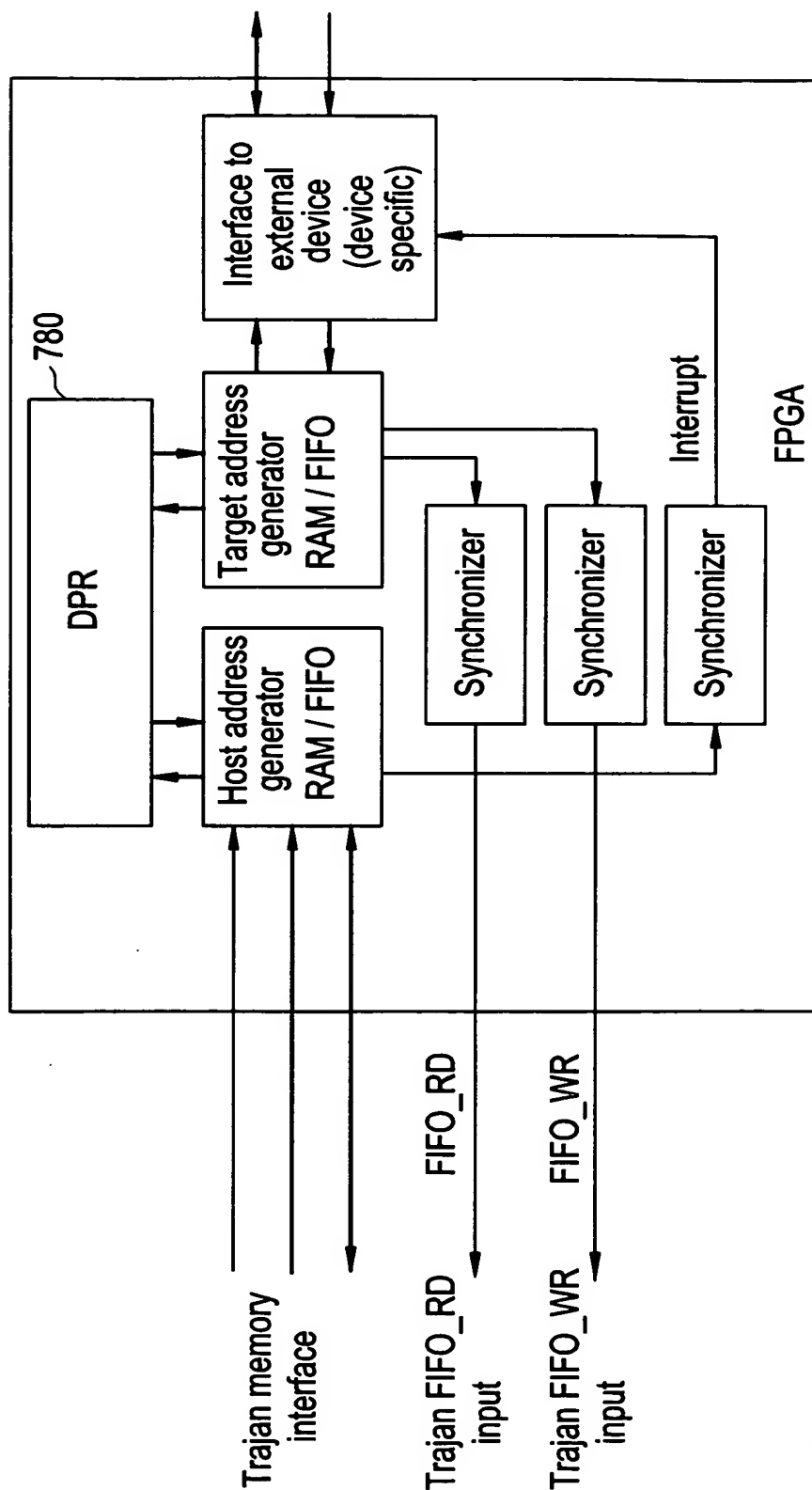




FIG. 68

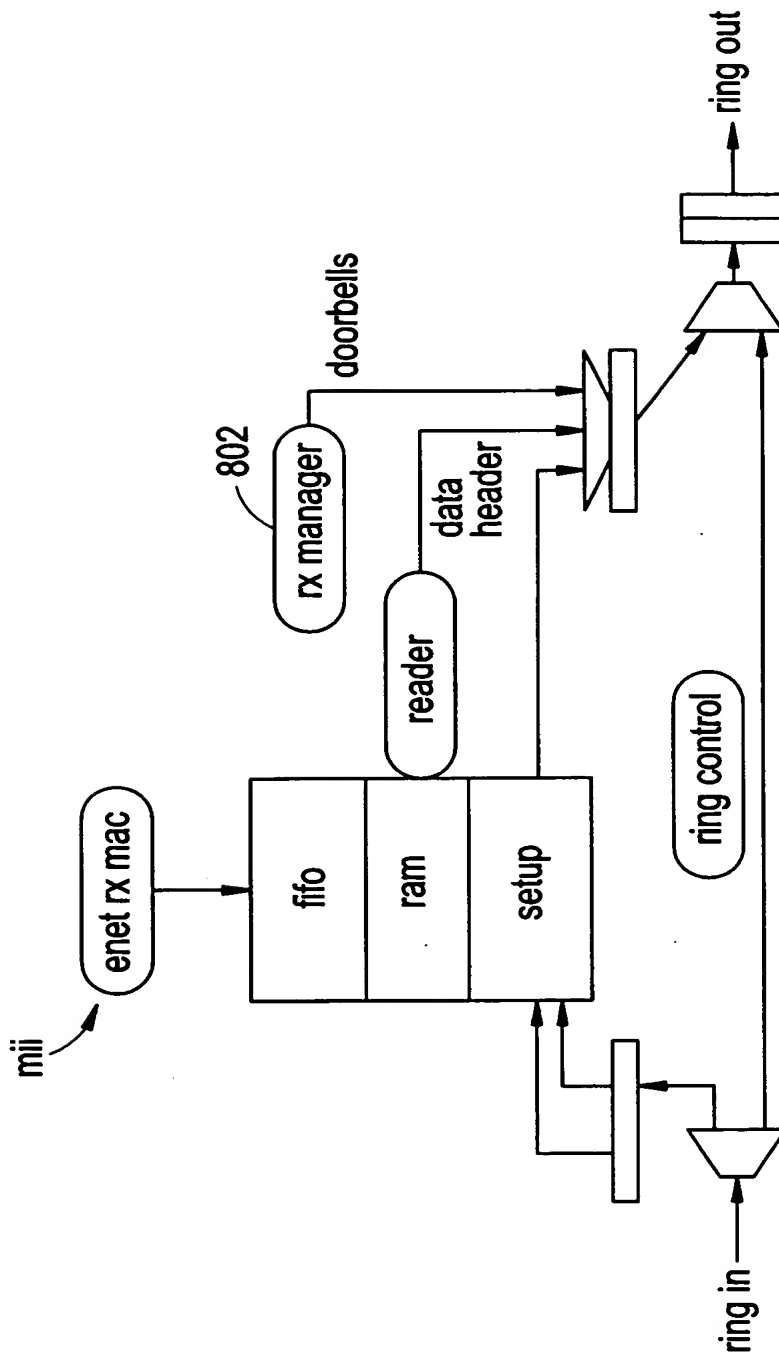
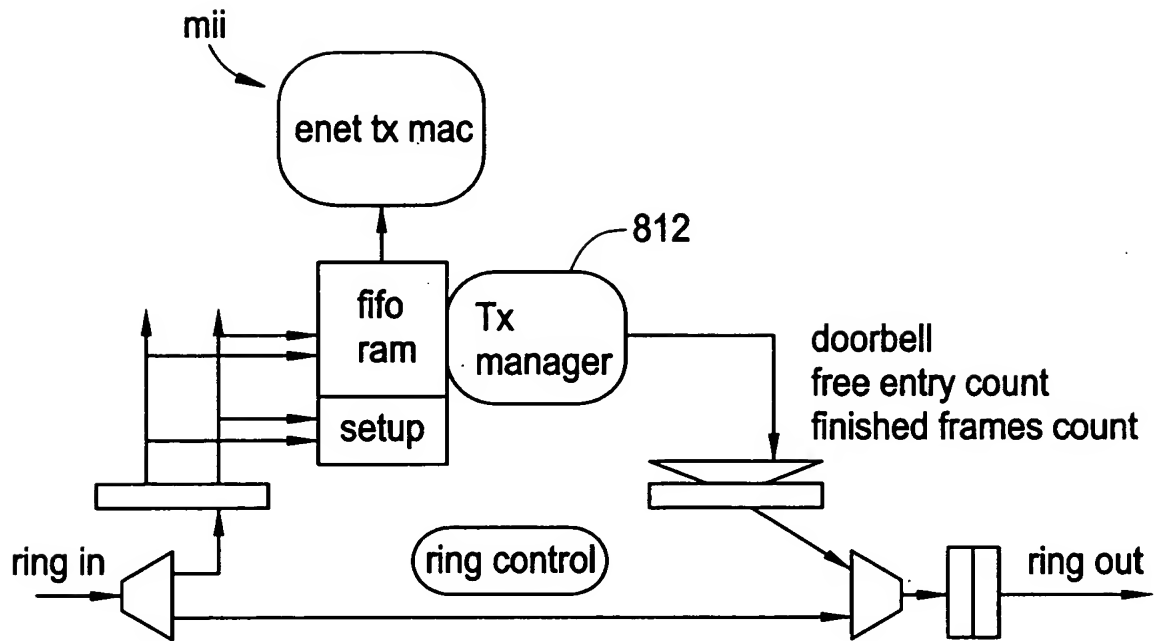


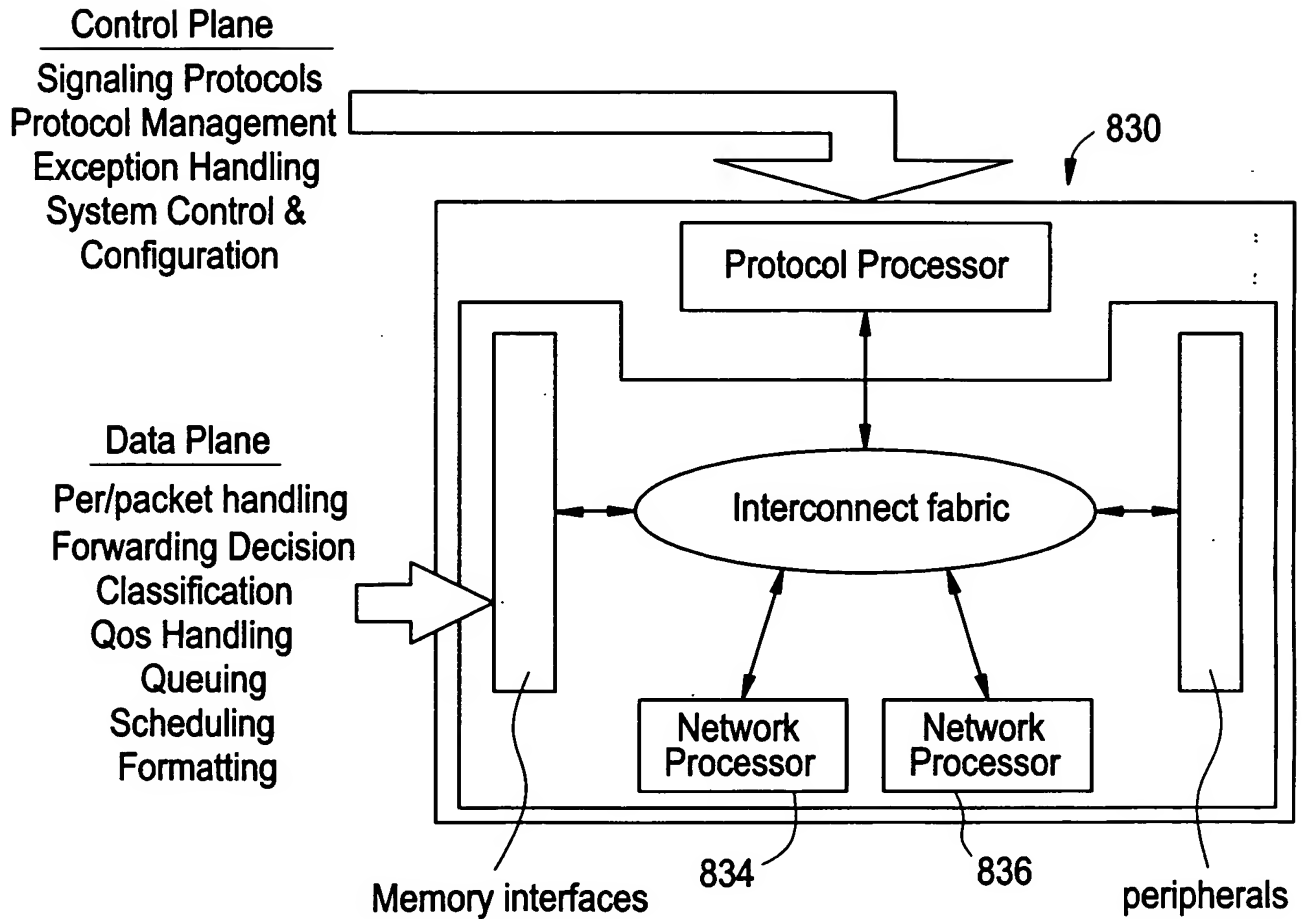
FIG. 69



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10064334.092602



FIG. 70



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FIG. 71

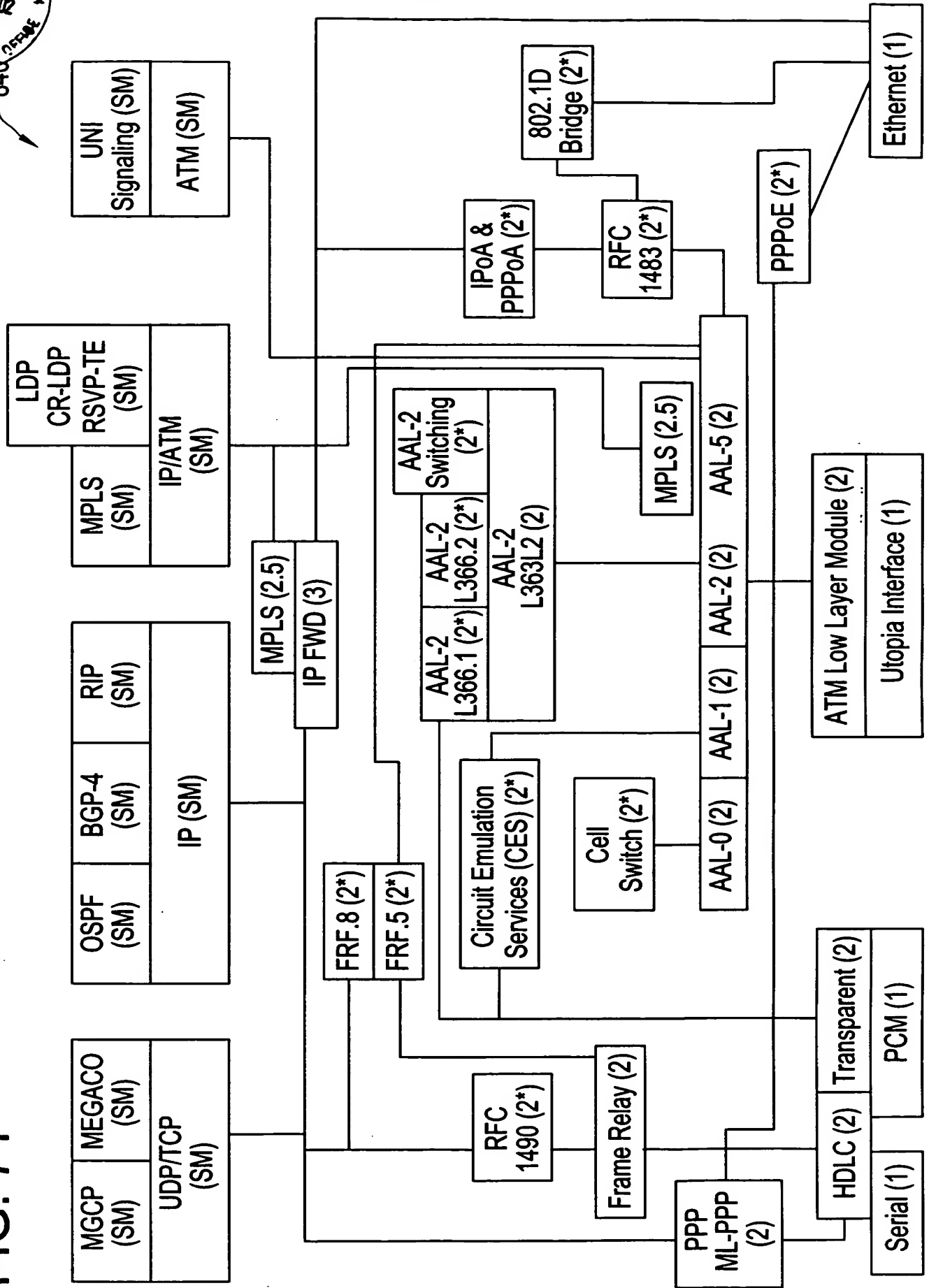
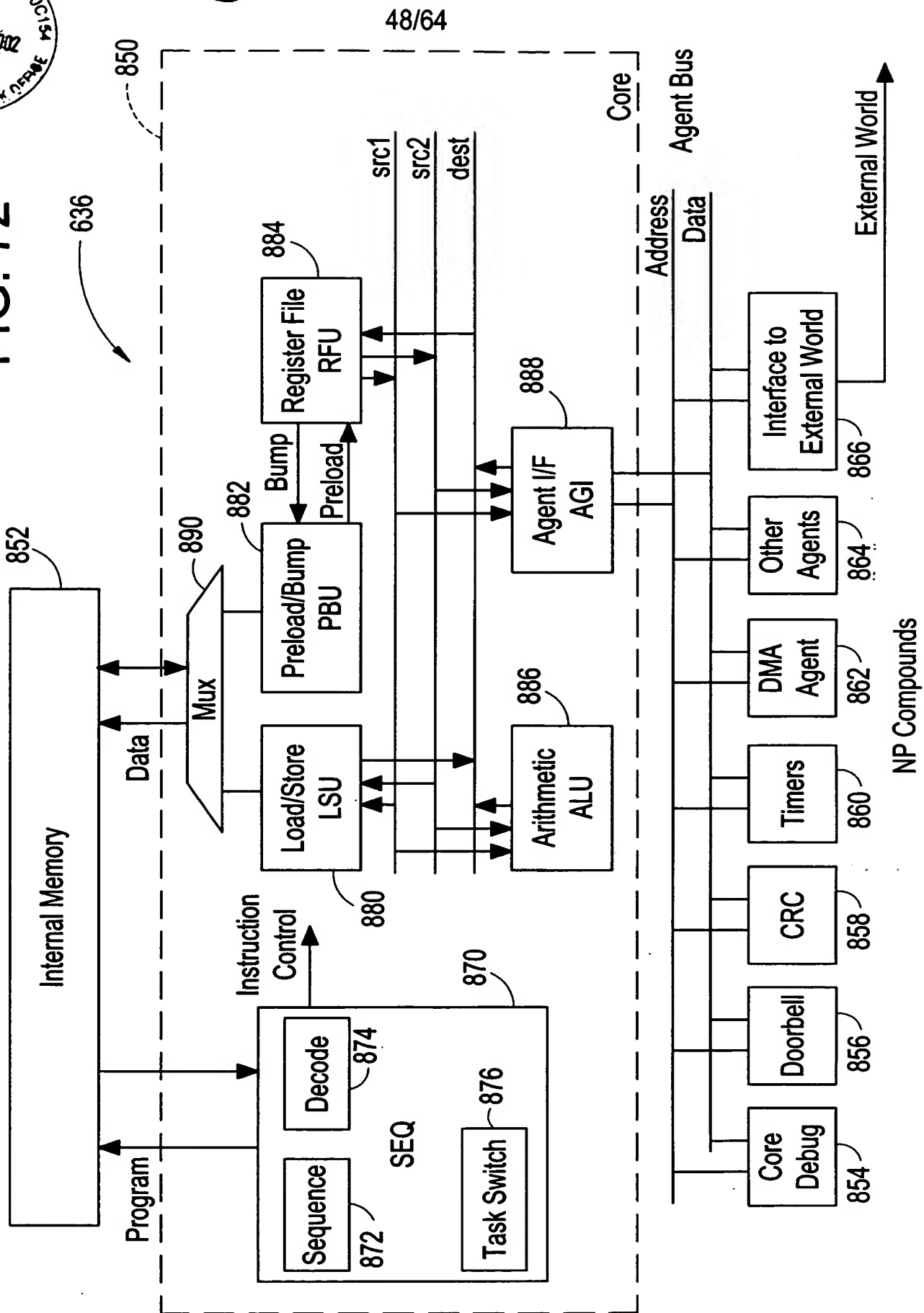




FIG. 72





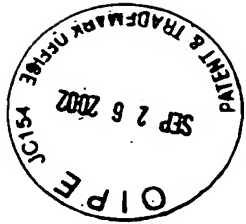
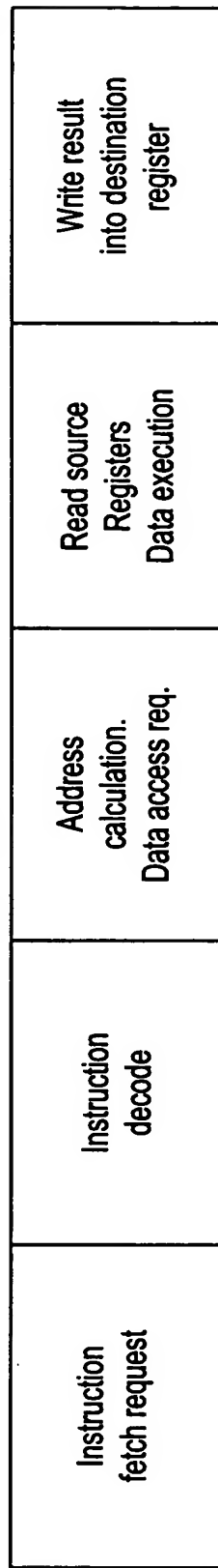
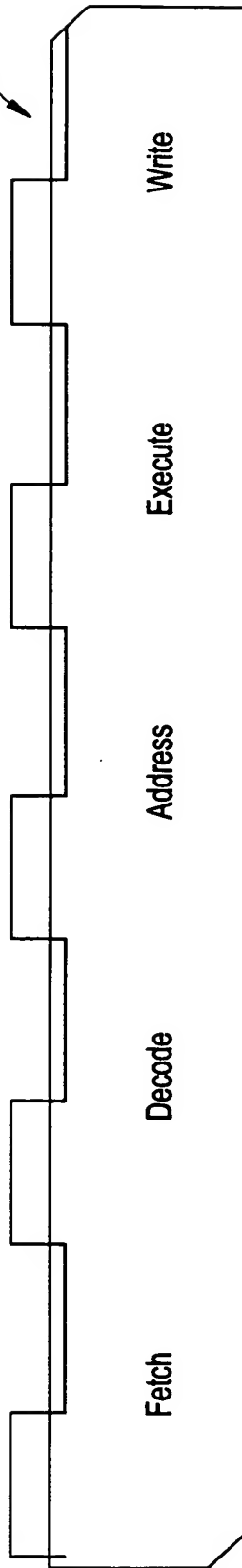
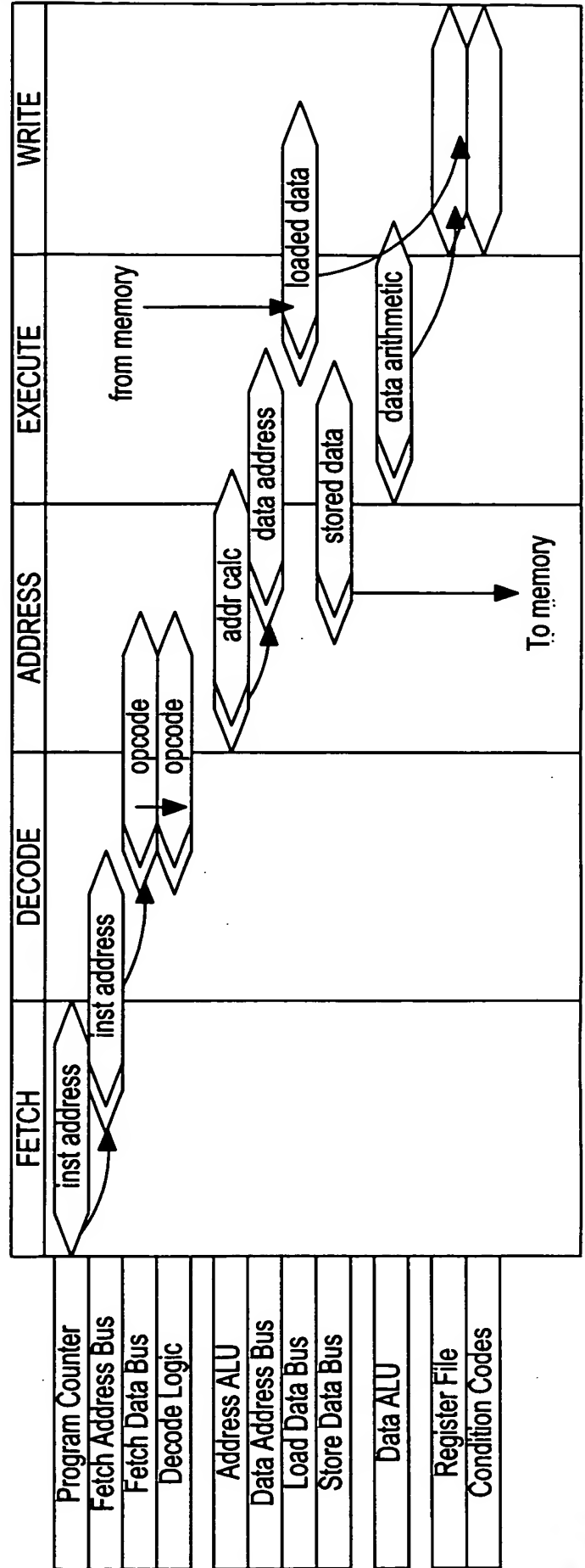


FIG. 73

900



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◊ - Flip Flop      ◊ - Logic

FIG. 74

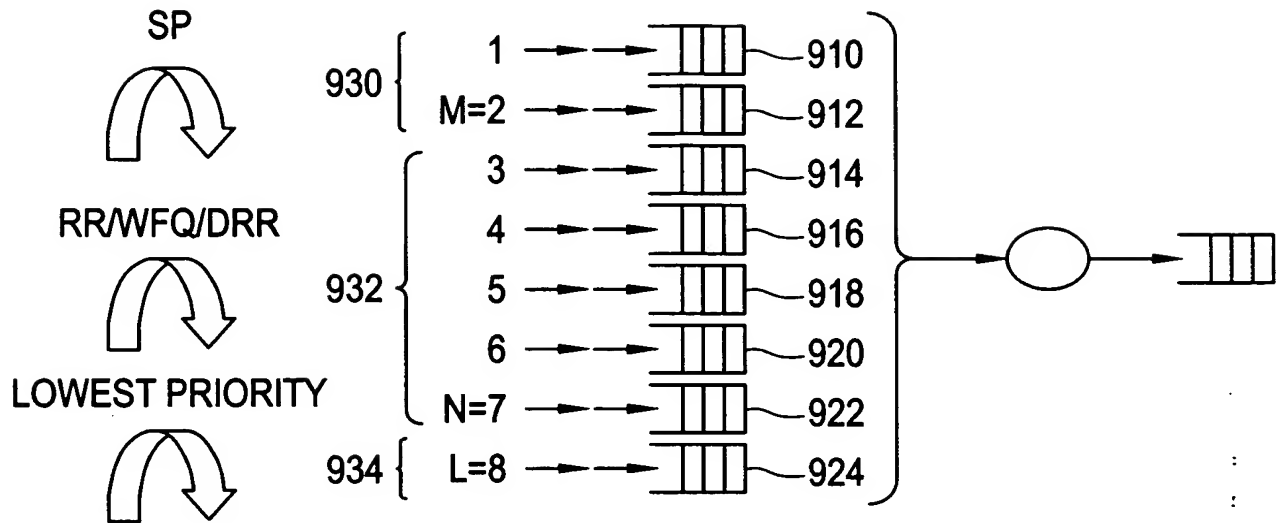
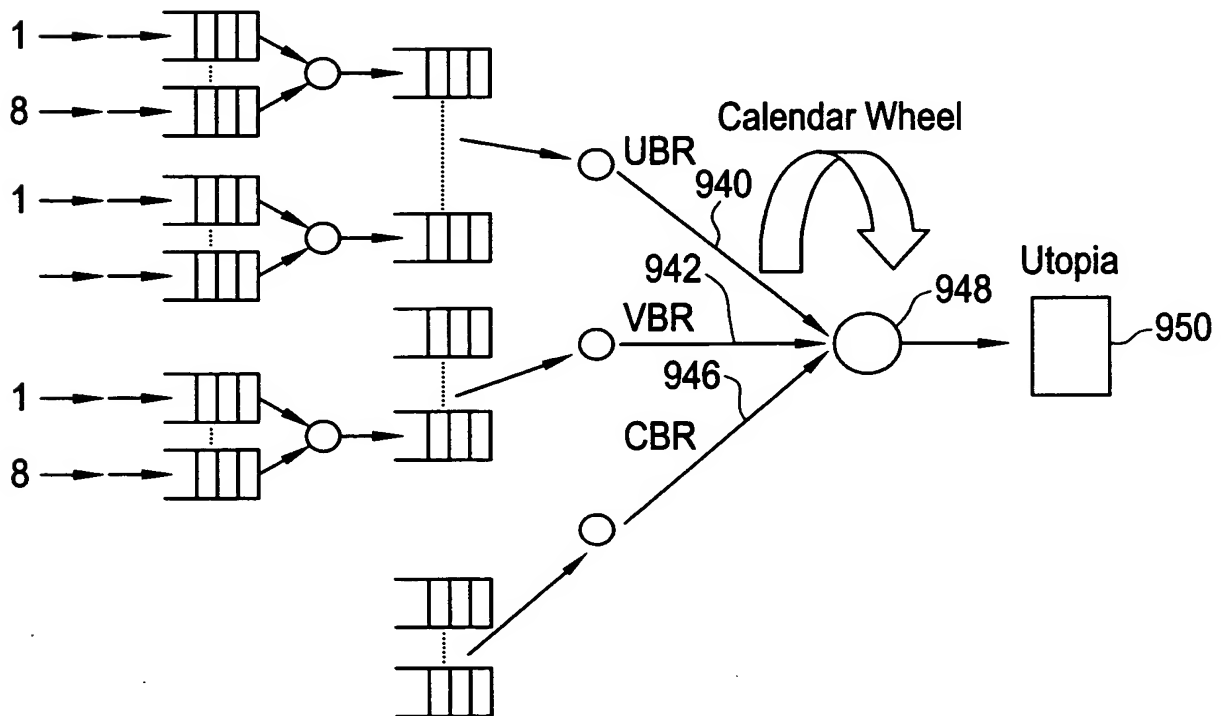


FIG. 75



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FIG. 76

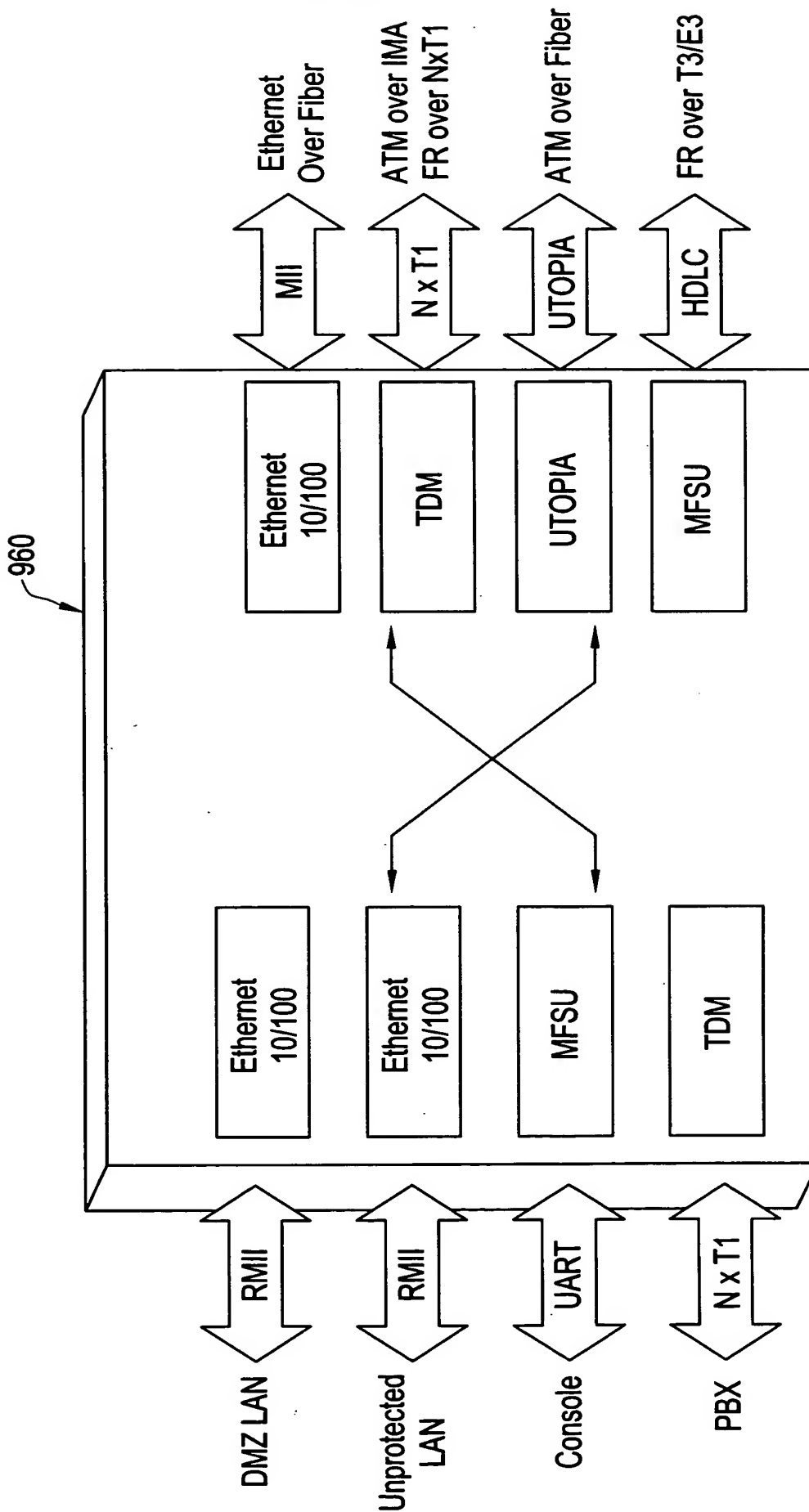


FIG. 77

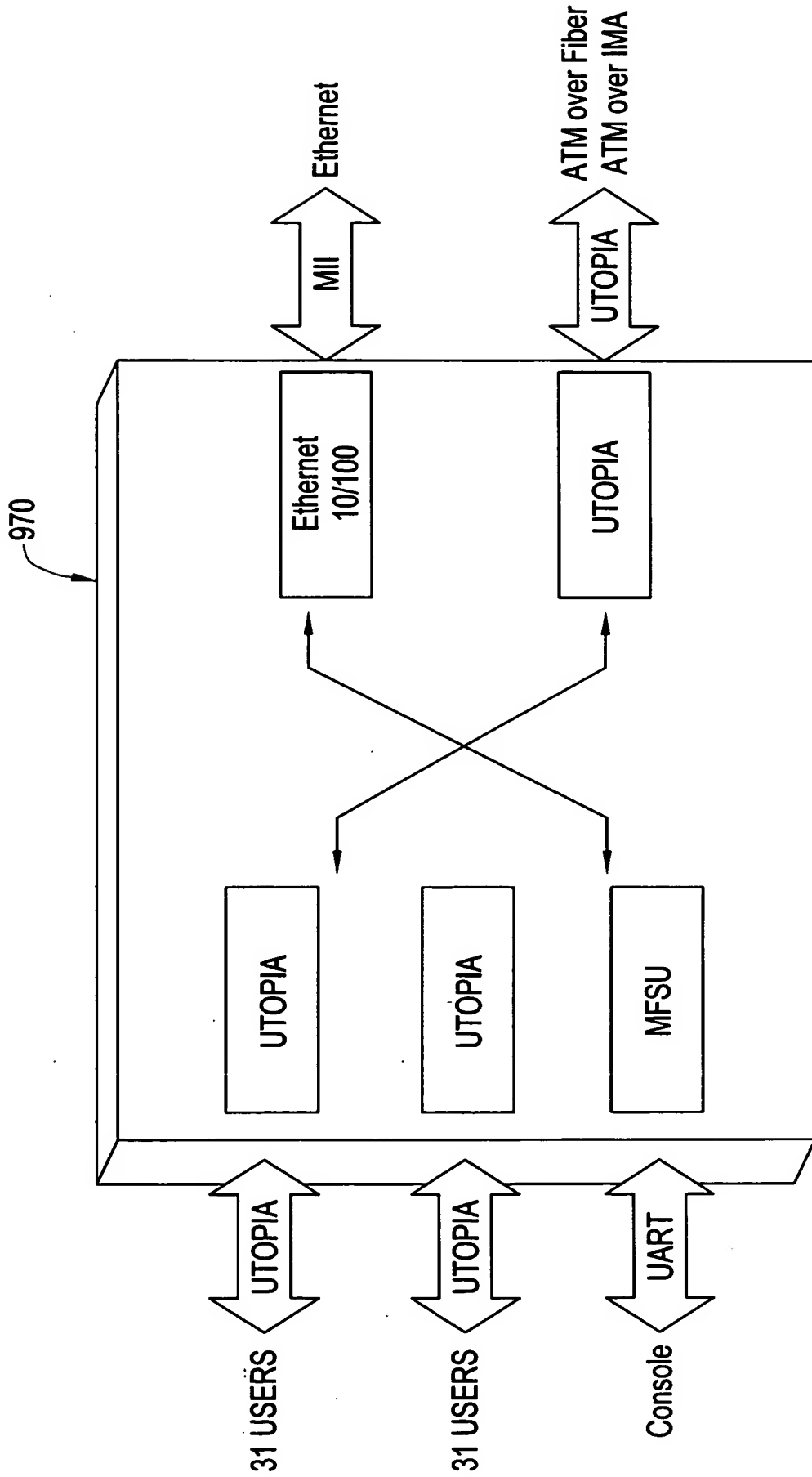




FIG. 78

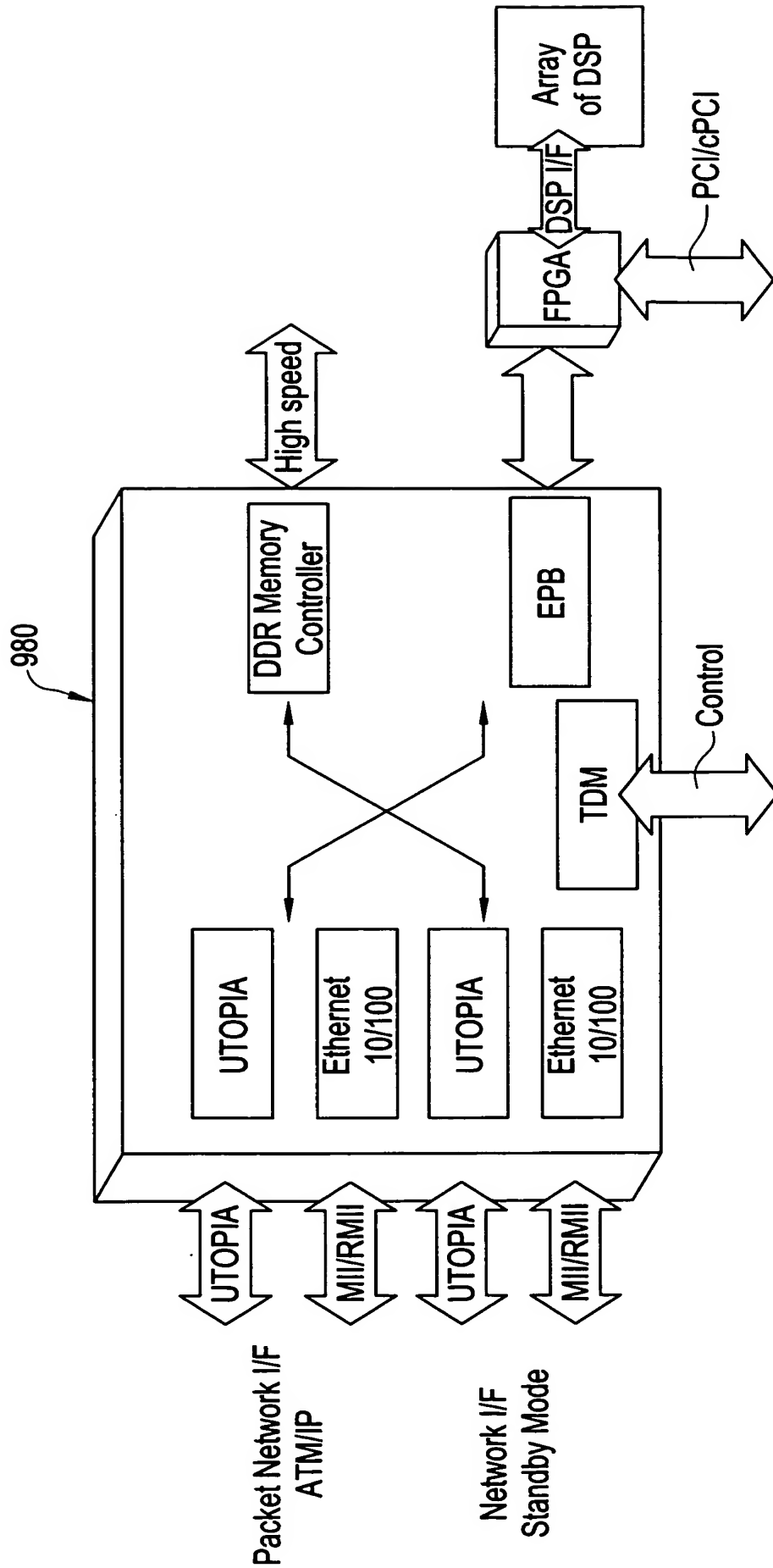


FIG. 79

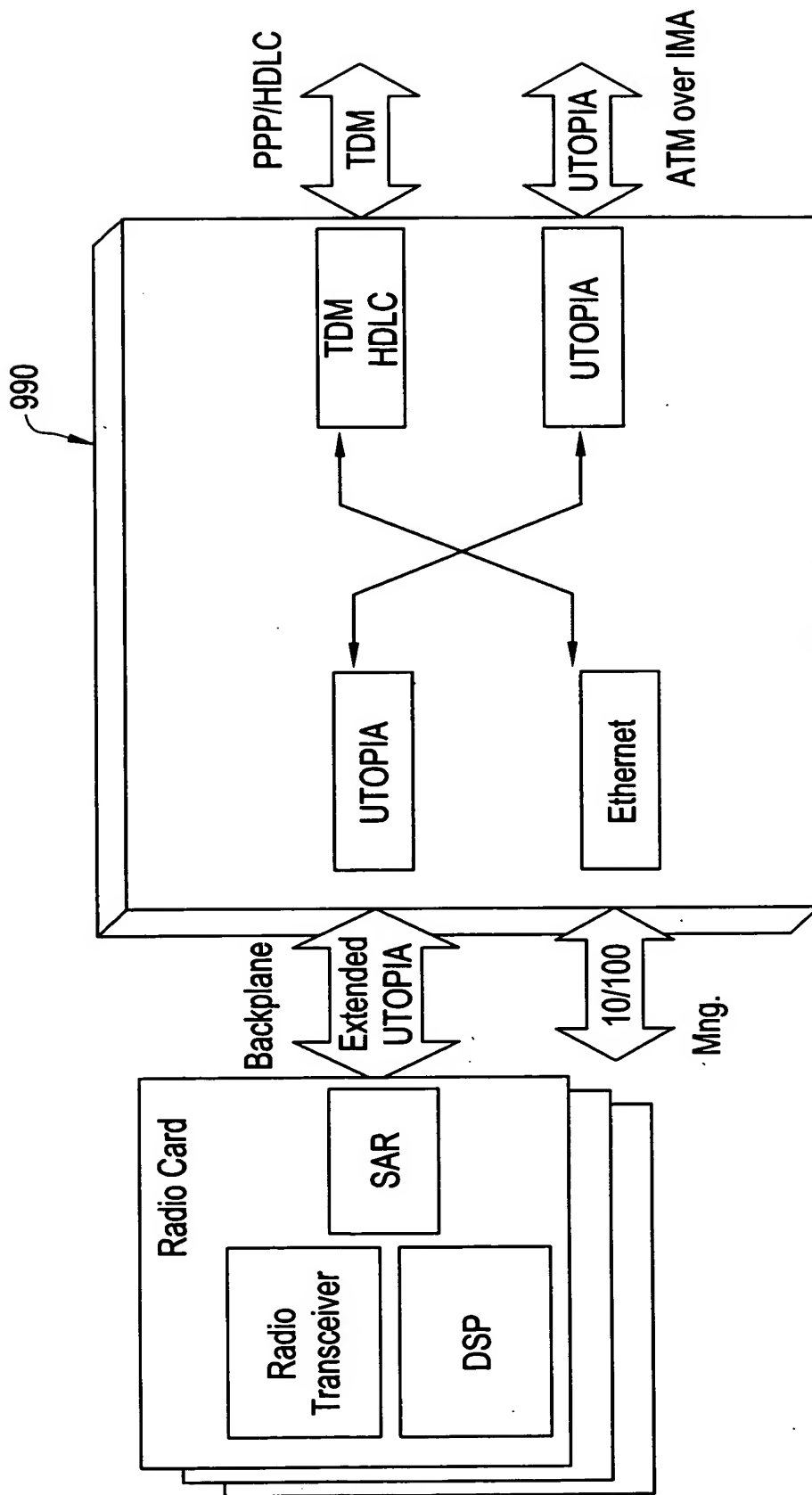
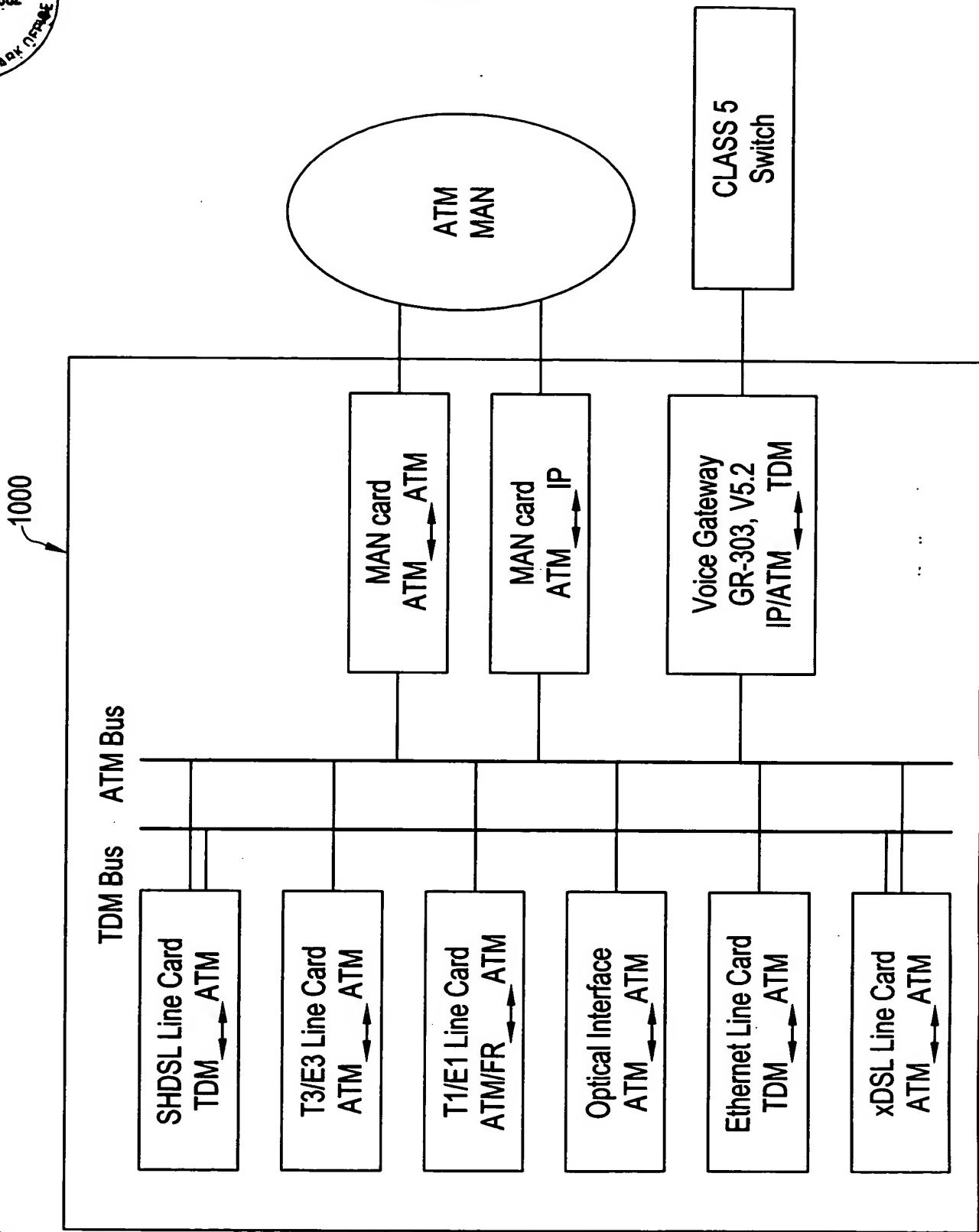


FIG. 80



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FIG. 81

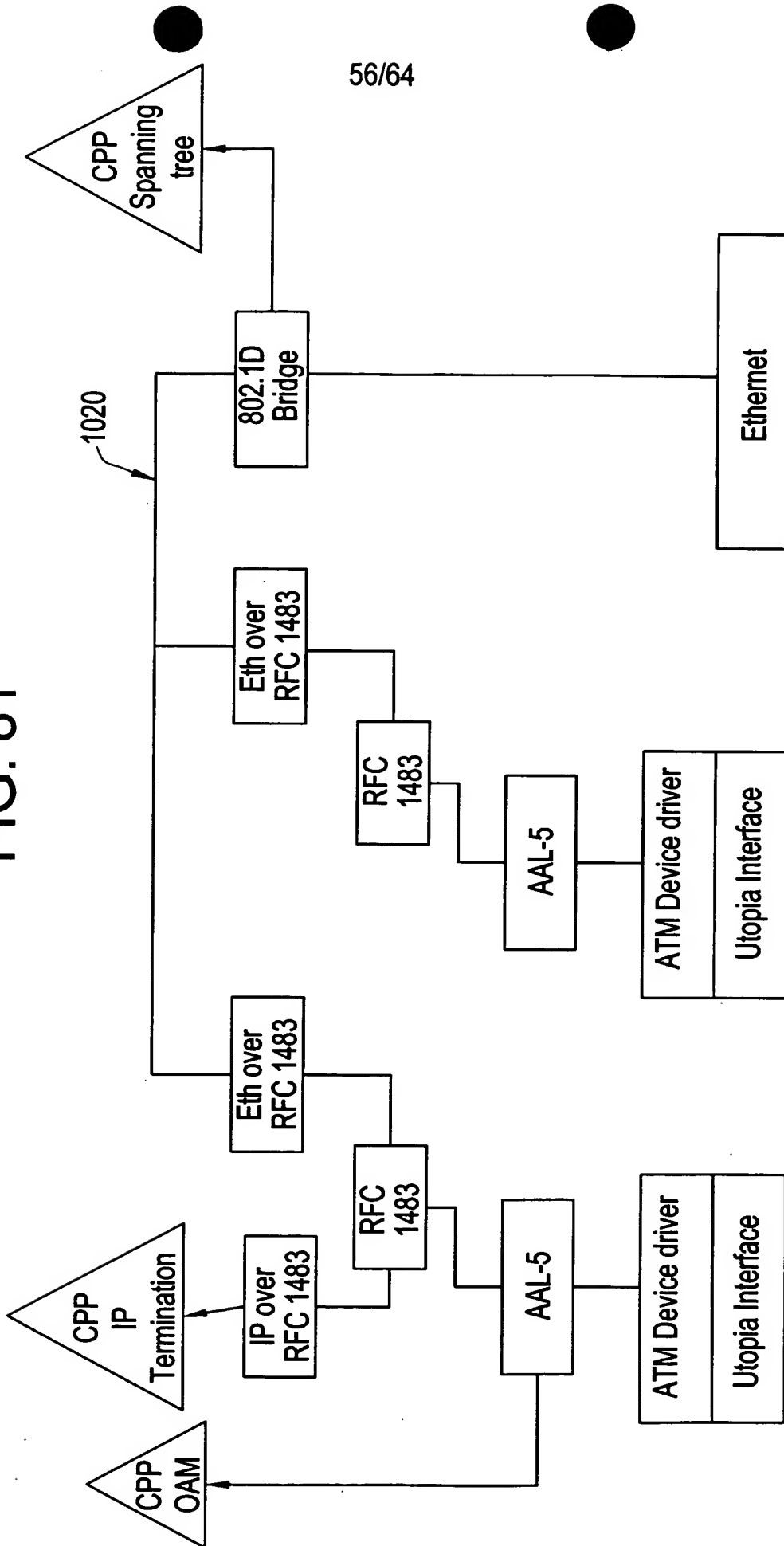




FIG. 82

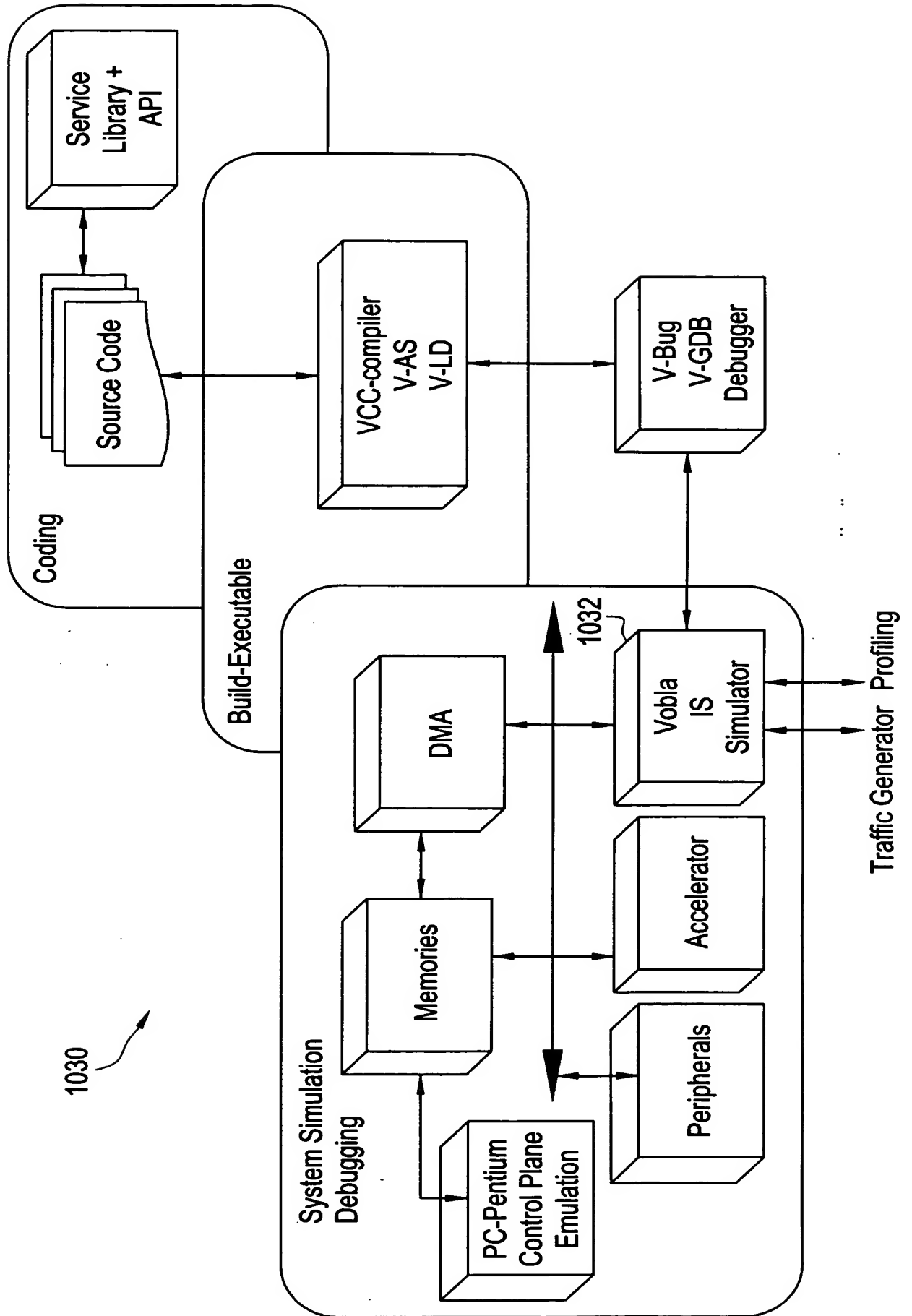


FIG. 83

1040

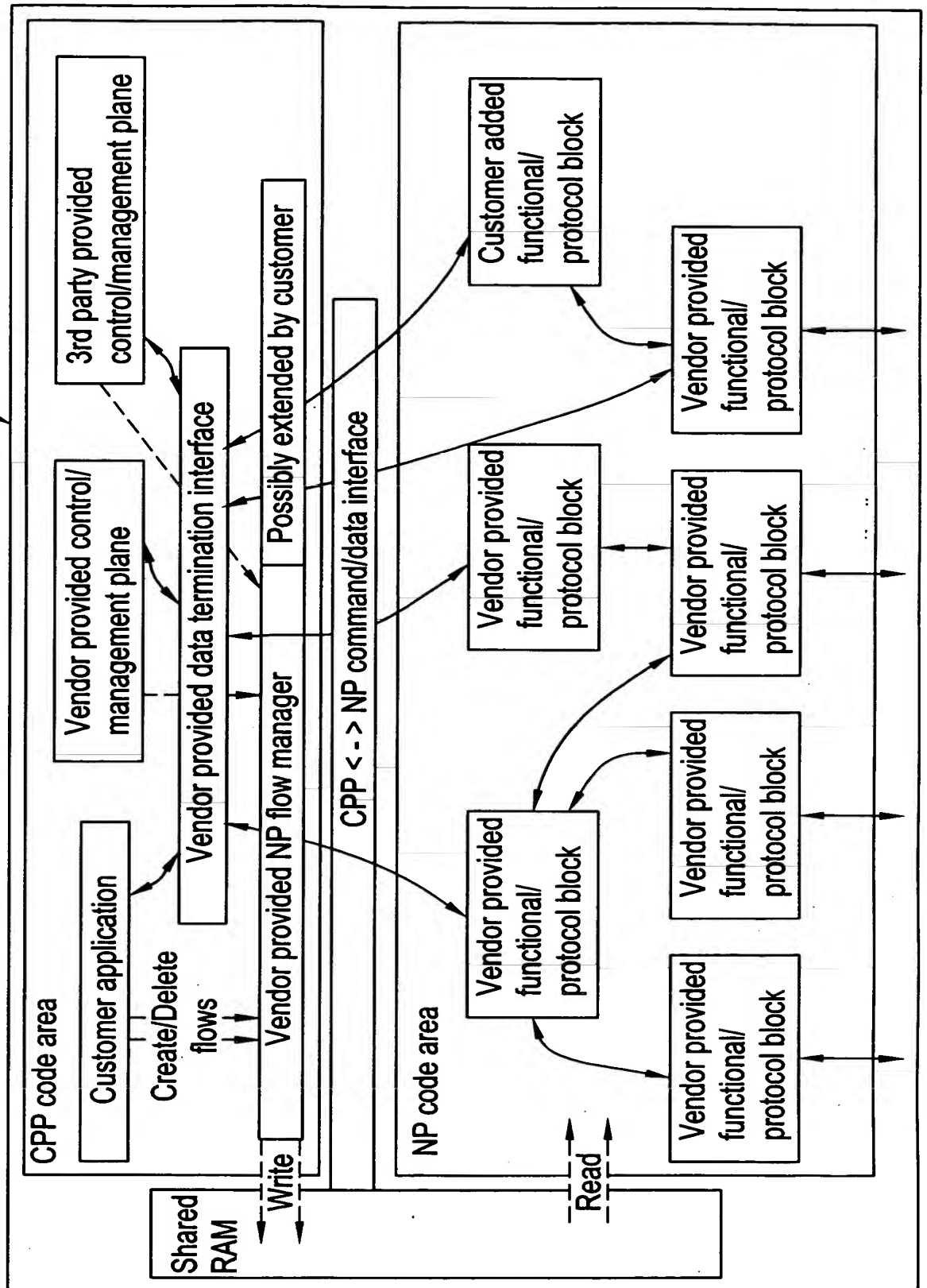
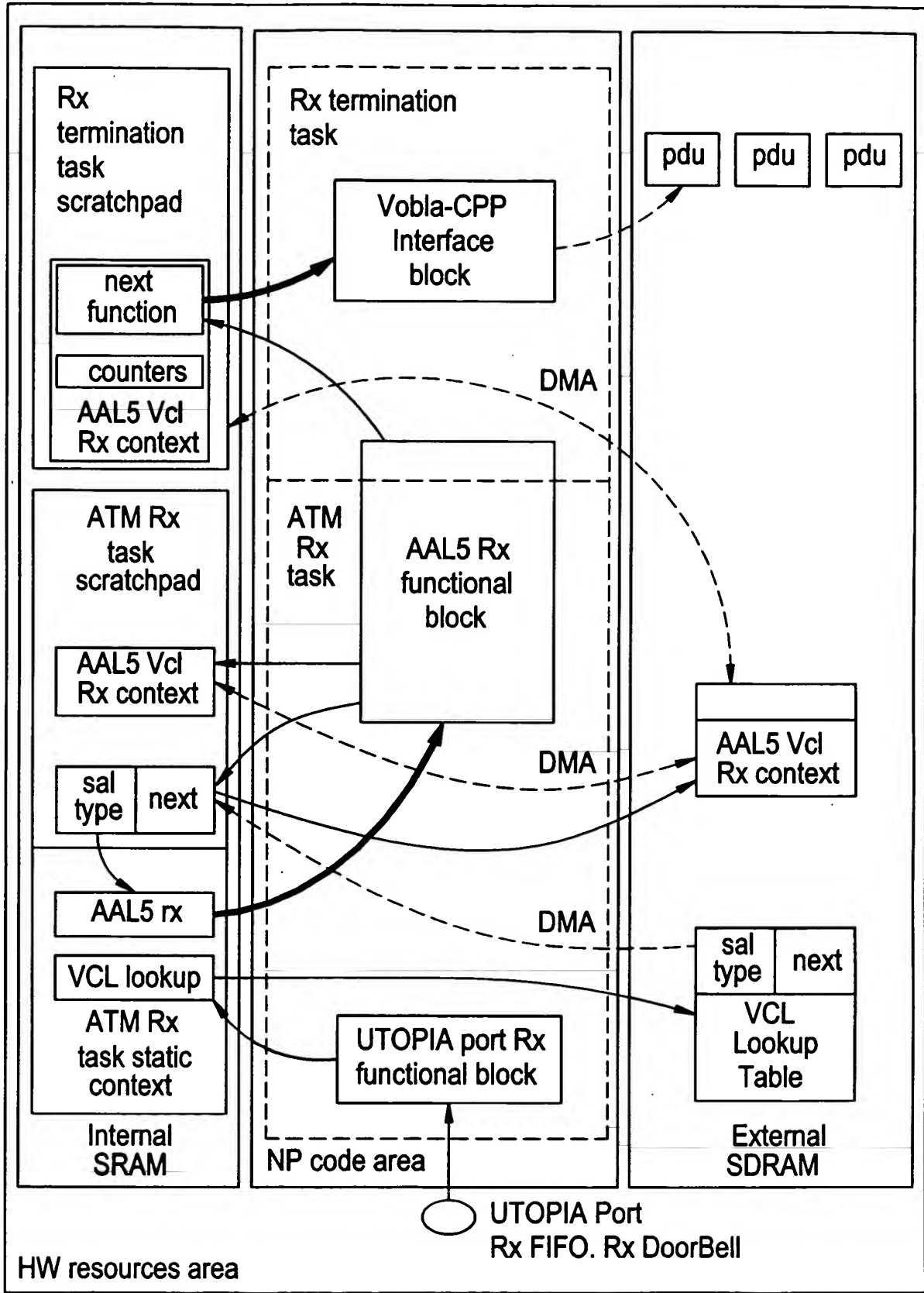


FIG. 84

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FIG. 85

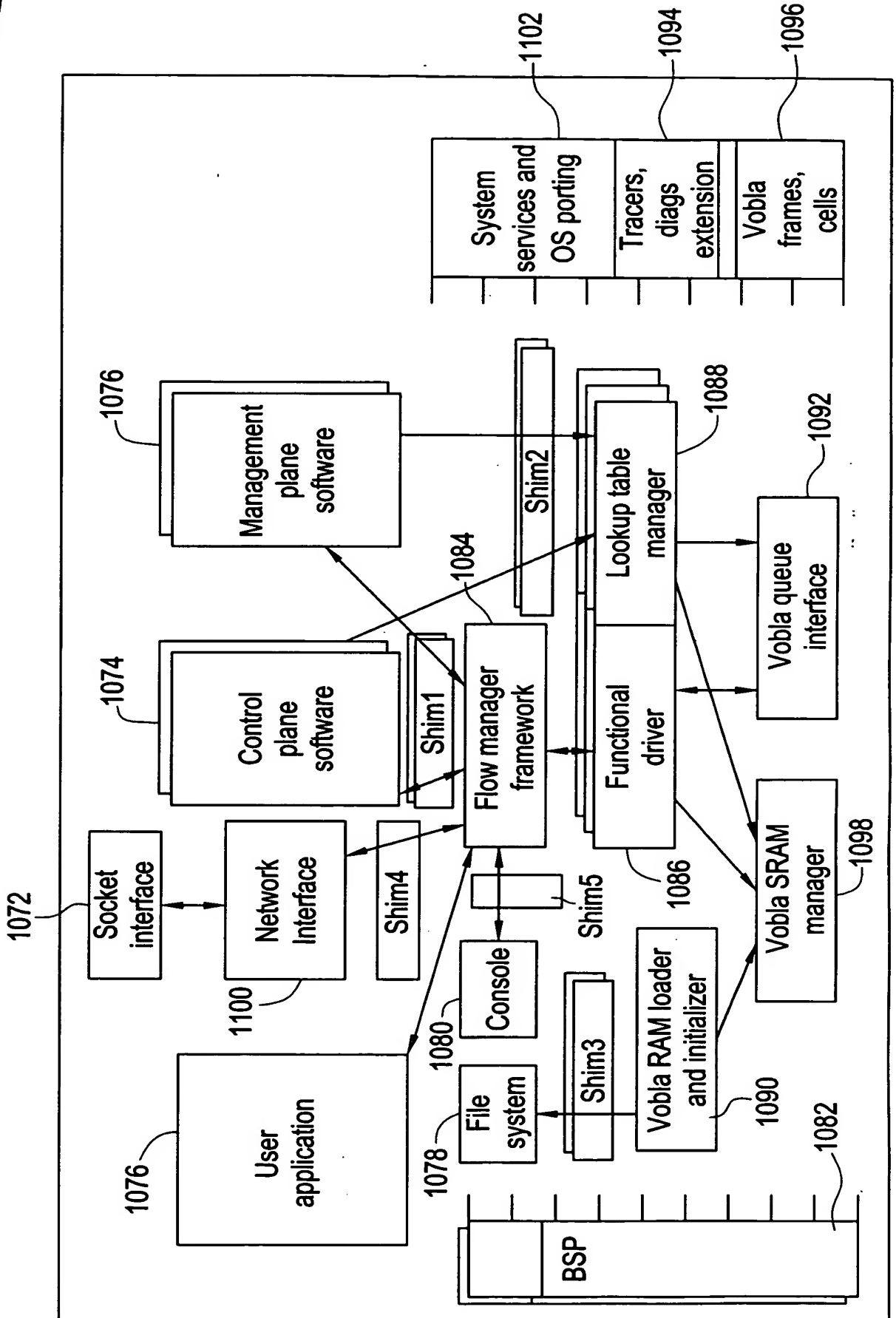
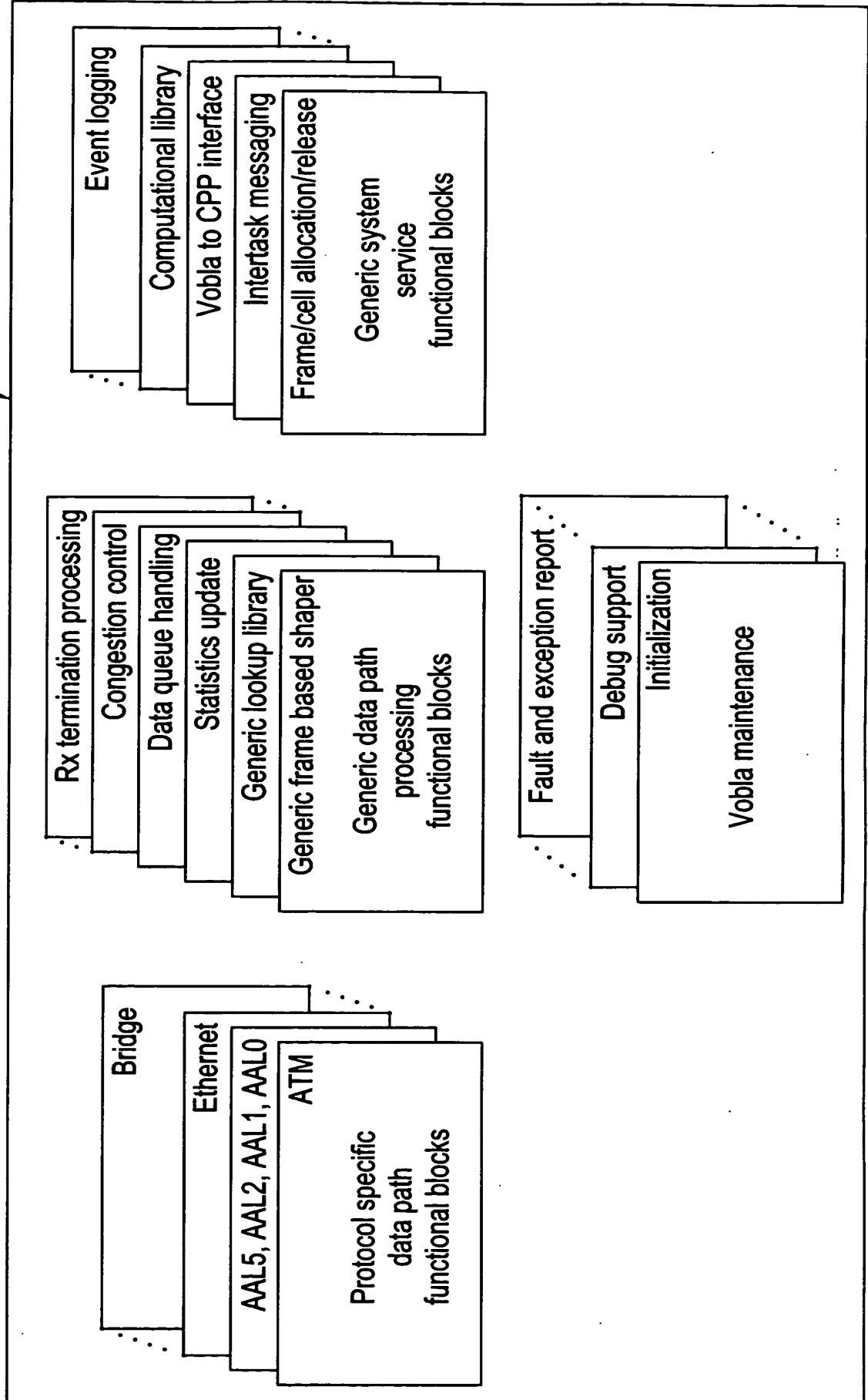


FIG. 86

1200

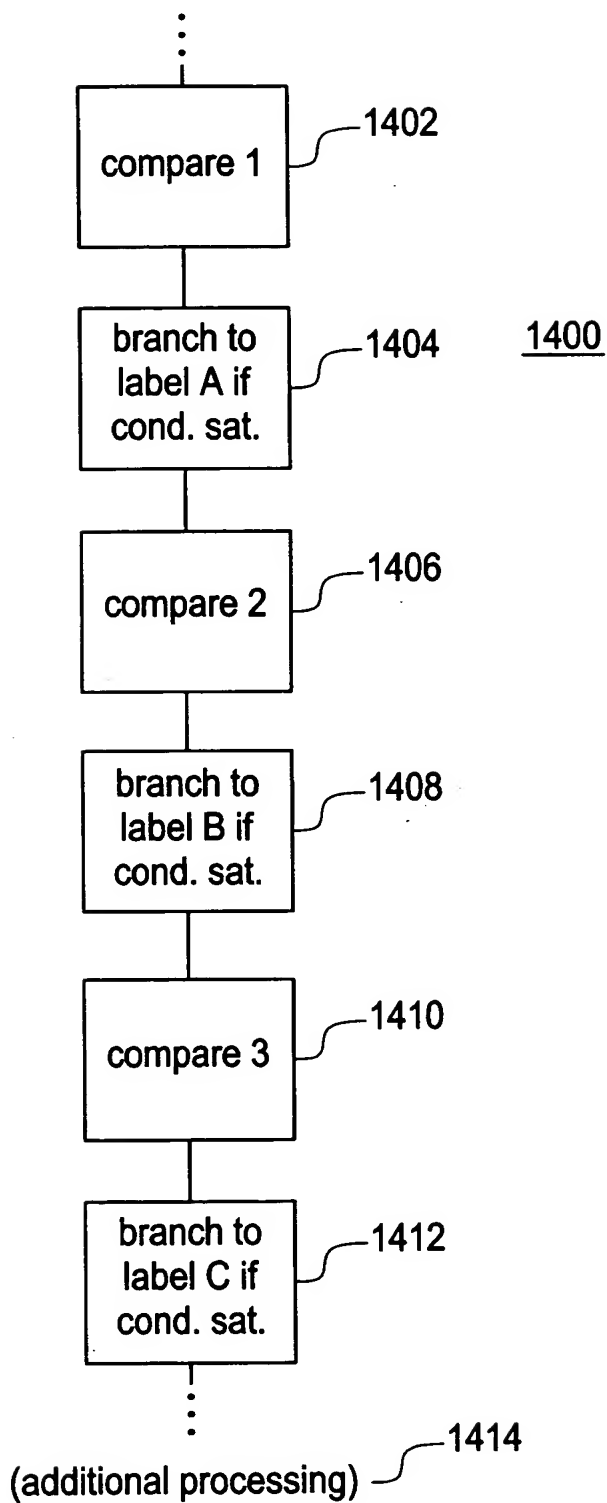




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# FIG. 87

PRIOR ART



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FIG. 88

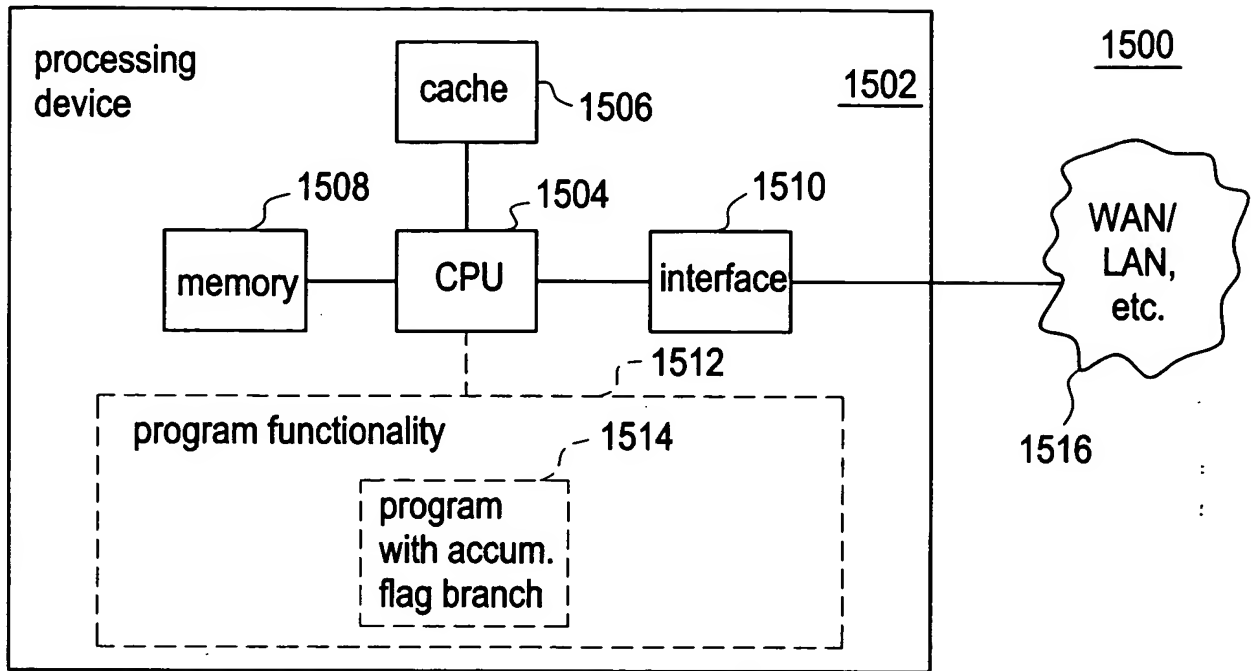


FIG. 89

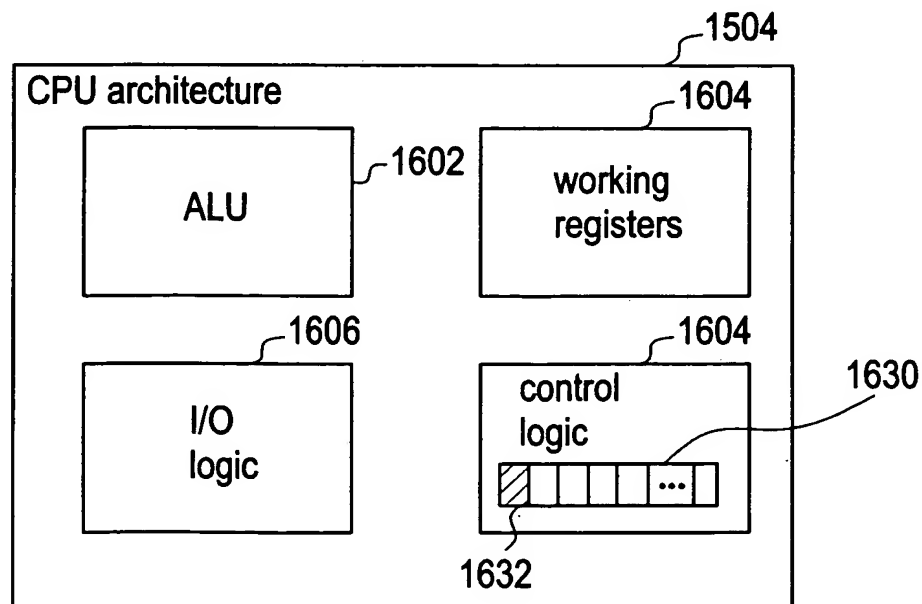
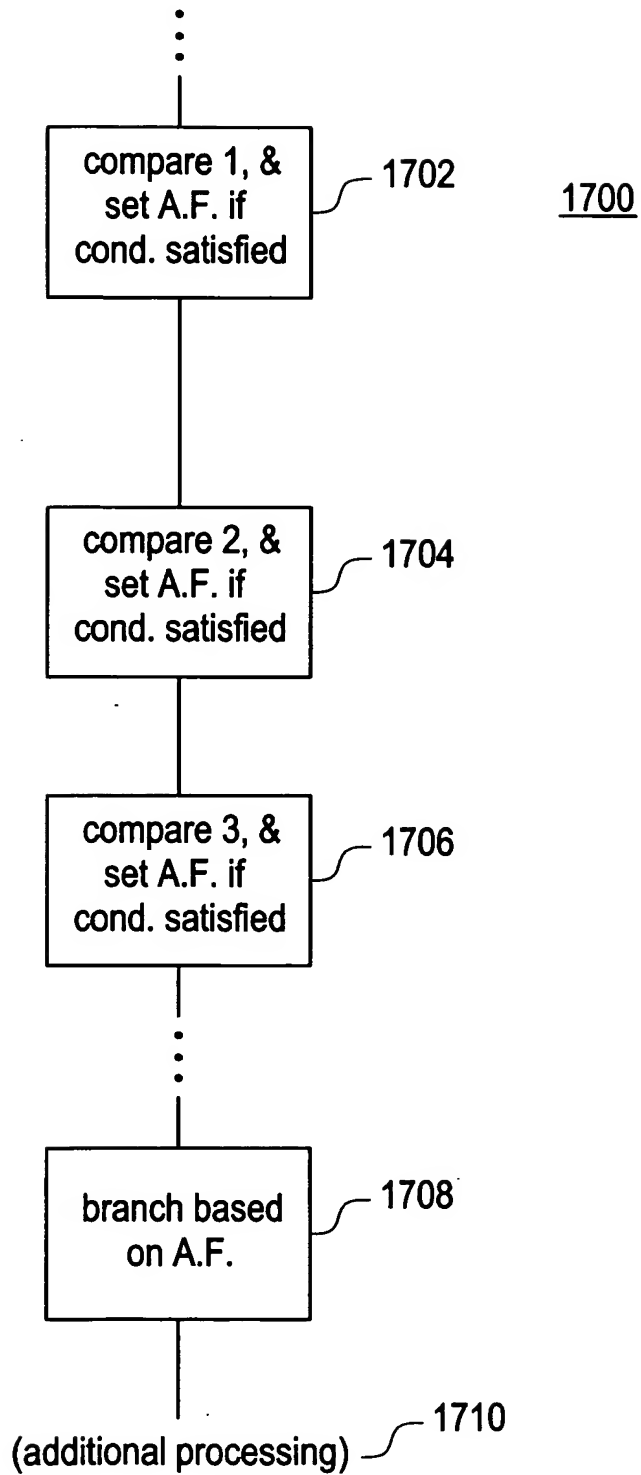


FIG. 90



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